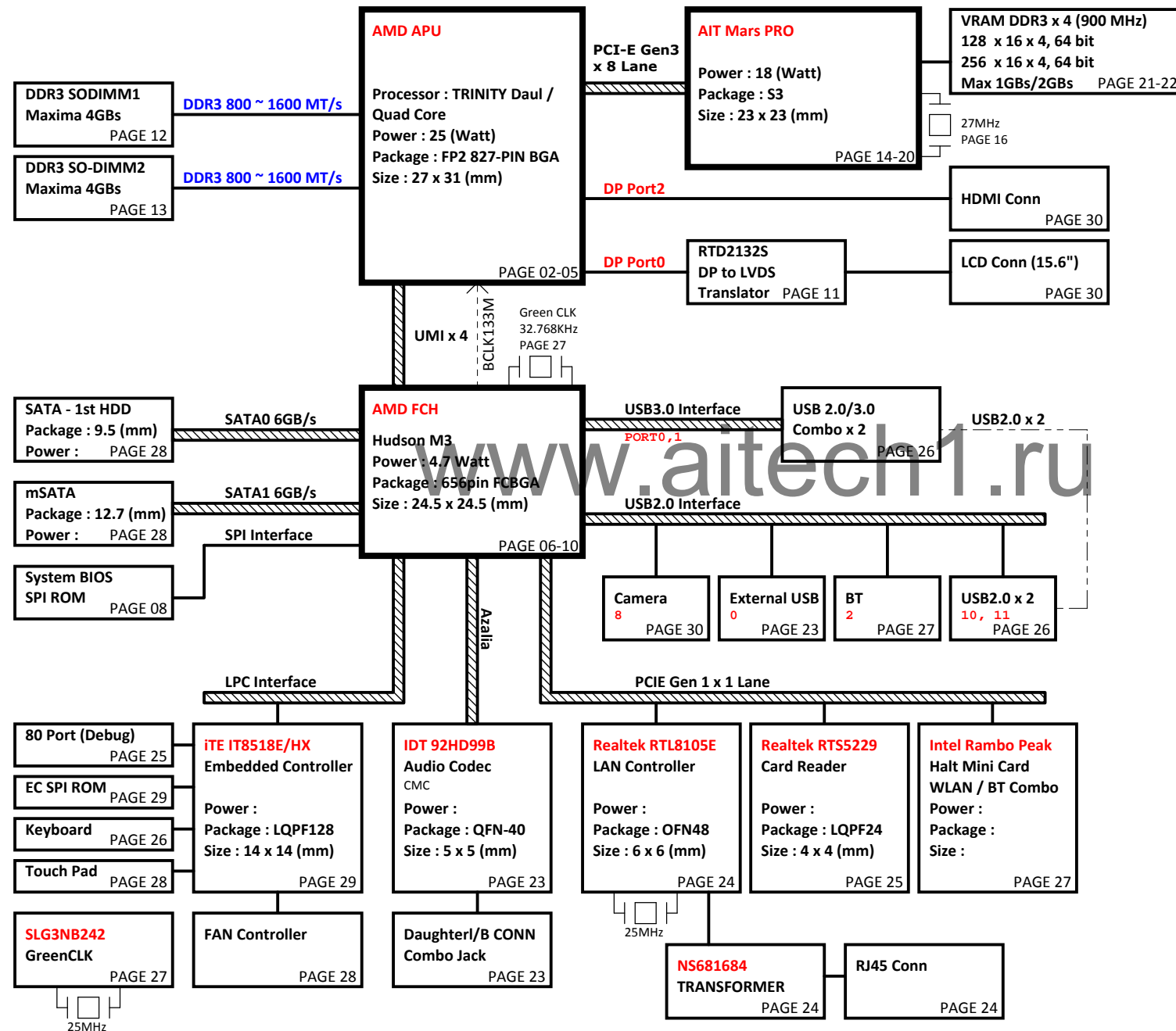


Tiguan1.0_AMD Comal DIS/UMA (15.6") Ultra/Slim 01





D

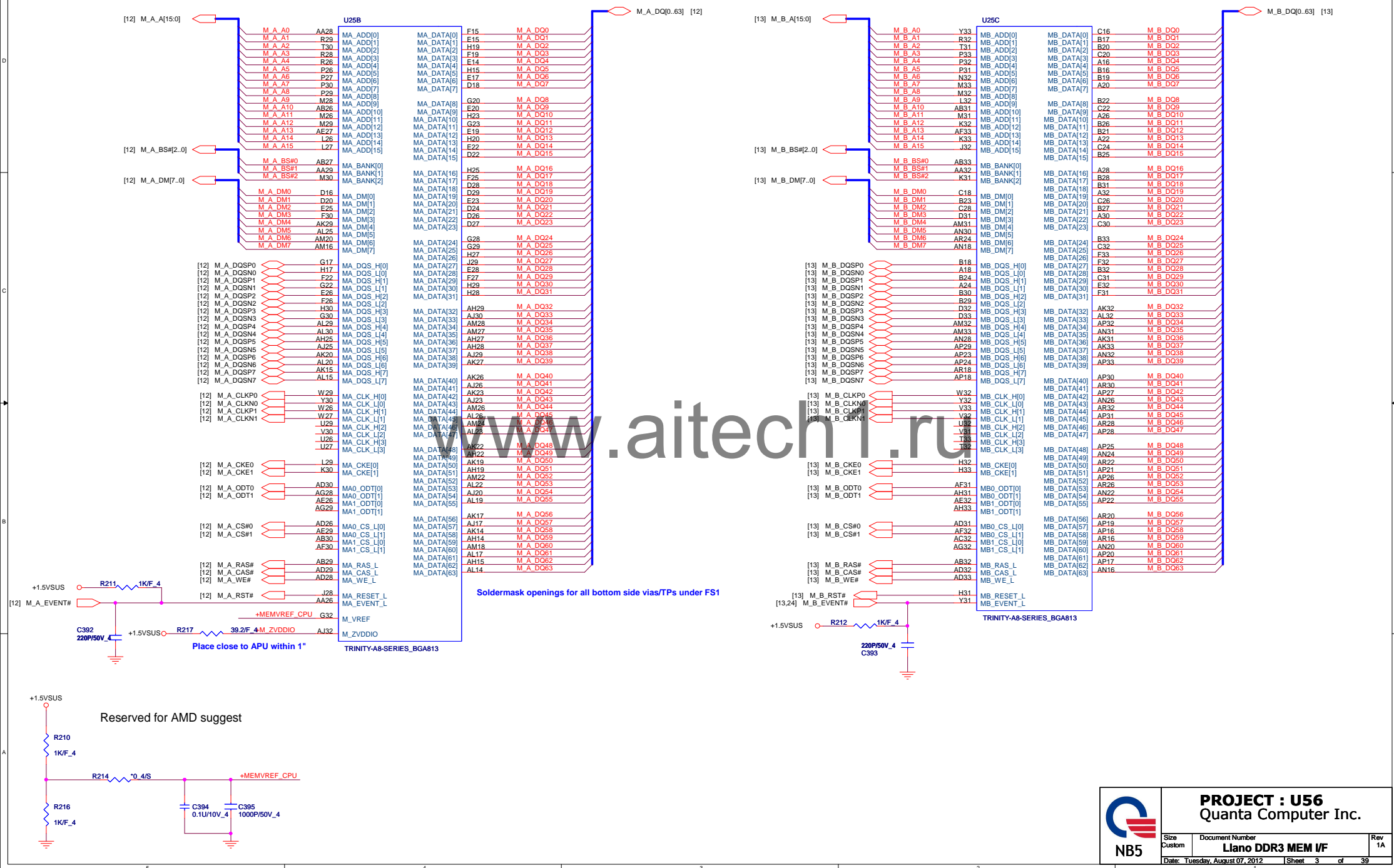


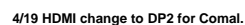
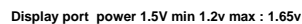
D

D

D





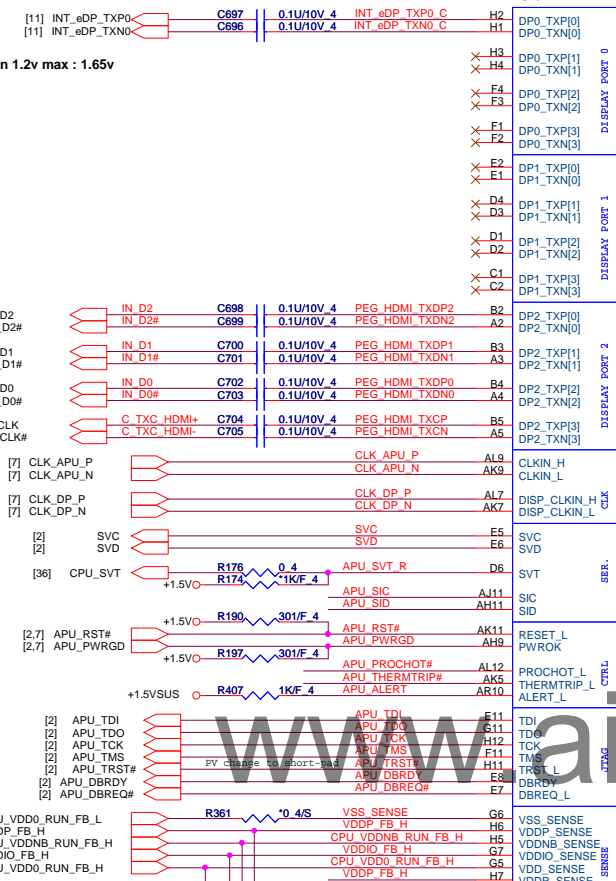


DP2 output to
HDMI connector

note -HDMI P&N can not swap

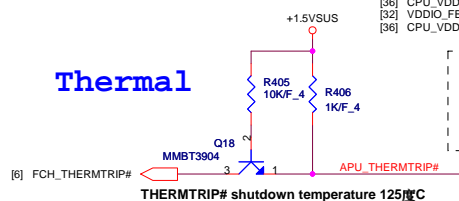
Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

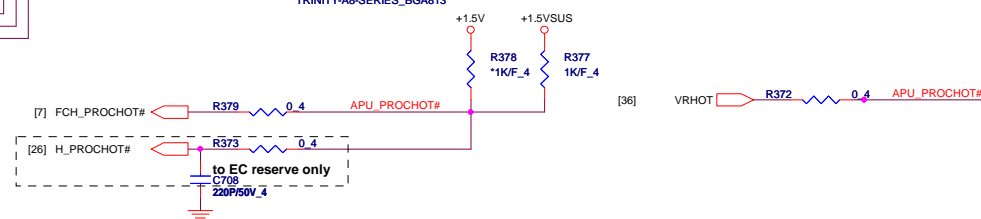


TRINITY-A8-SERIES_BGA813

Thermal



4/19 For Comal,
close to APU.

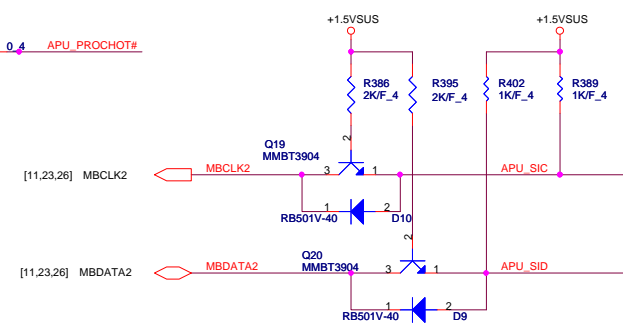
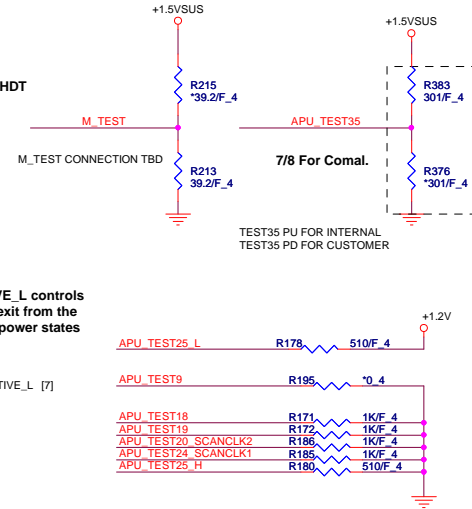


over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C




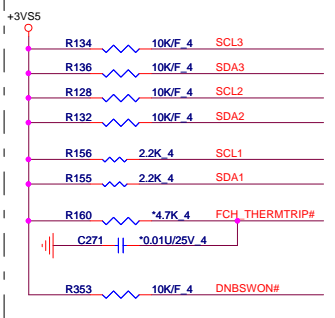
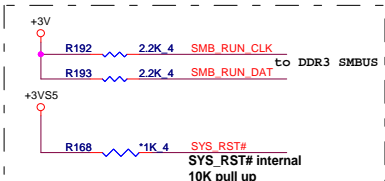
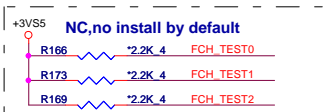
DMAACTIVE_L controls entry and exit from the sleep and power states



PROJECT : U56
Quanta Computer Inc.

Size	Document Number Llano Display/Misc	Revision 1A
Date:	Tuesday, August 07, 2012	Sheet 4 of 39

 NB5	PROJECT : U56 Quanta Computer Inc.		
	Size Custom	Document Number Llano POWER/GND	Rev 1A
	Date: Wednesday, July 11, 2012 Sheet 5 of 39		



GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V

GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3V55

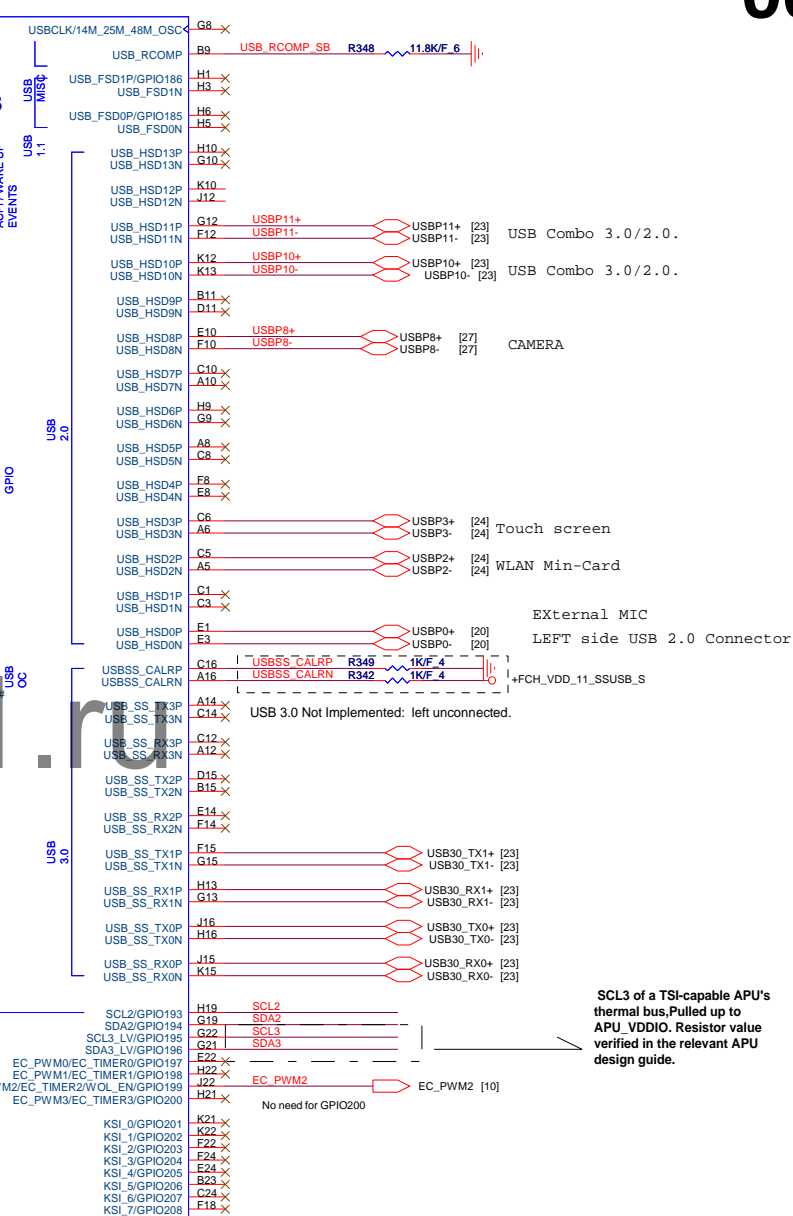
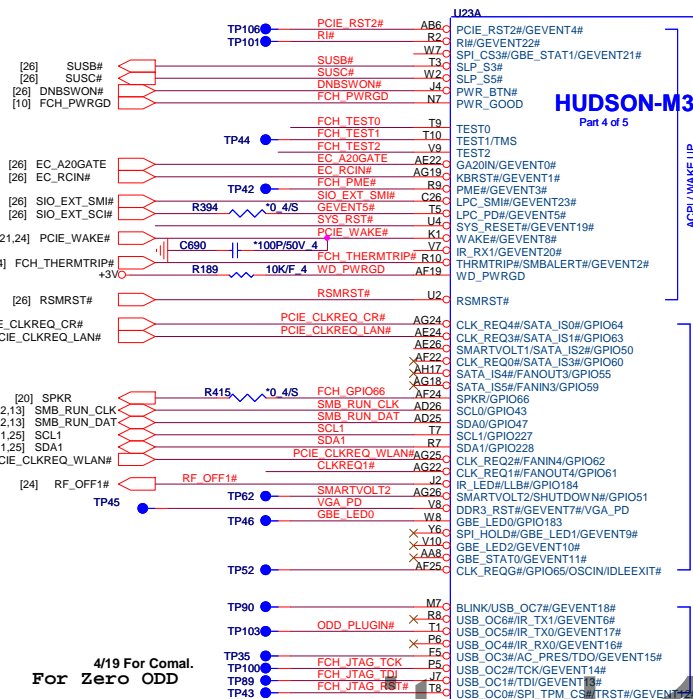
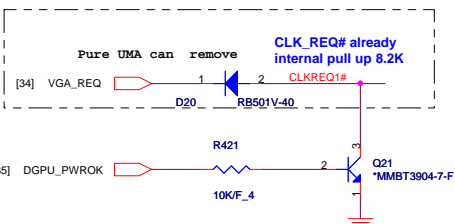
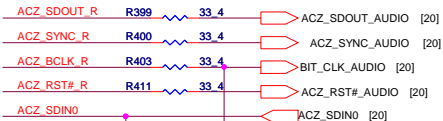
PCIE_WAKE# no need to pull
Hi resistor from check list

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

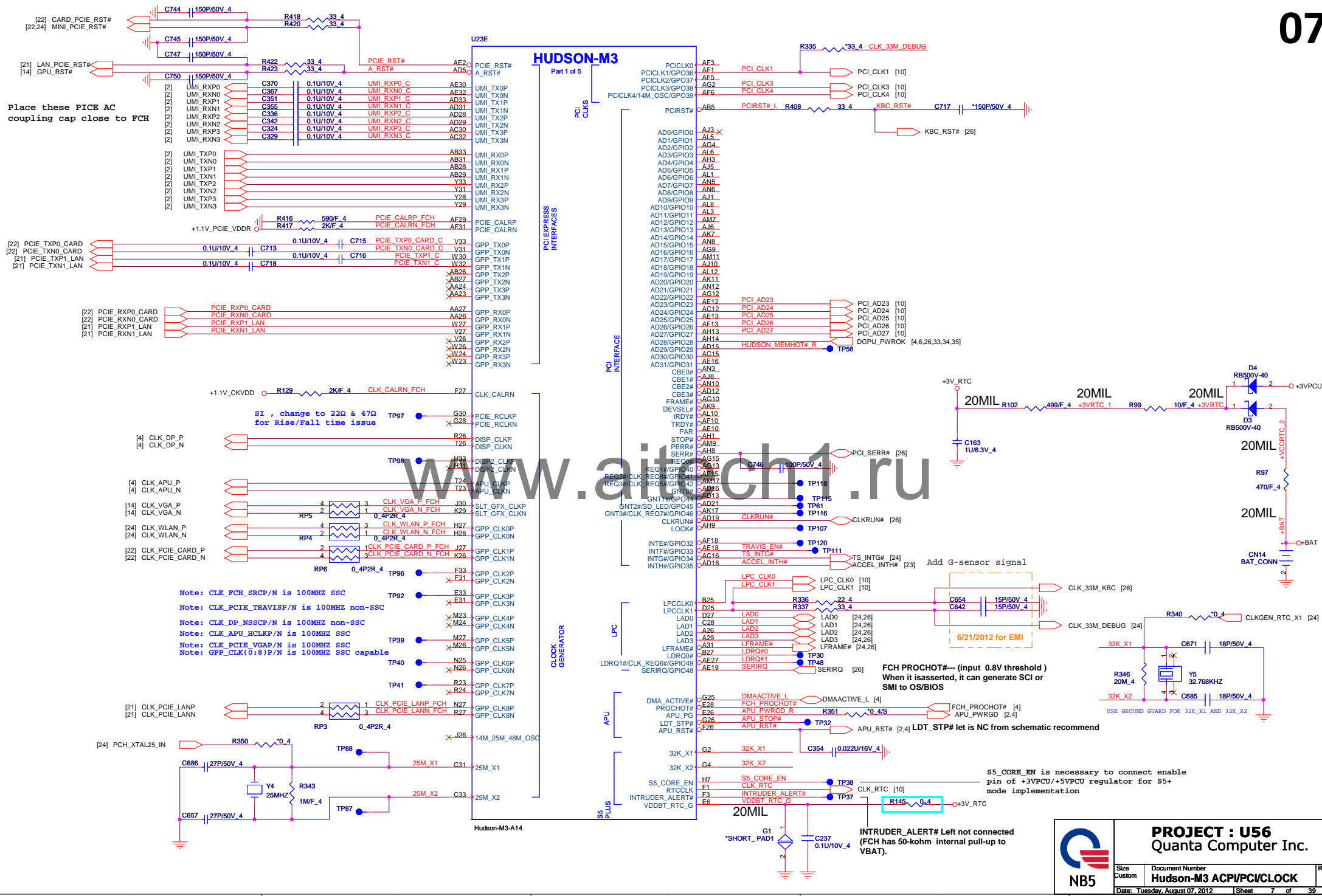
This pin is used to
power down VGA DAC
regulators when CRT
no connected

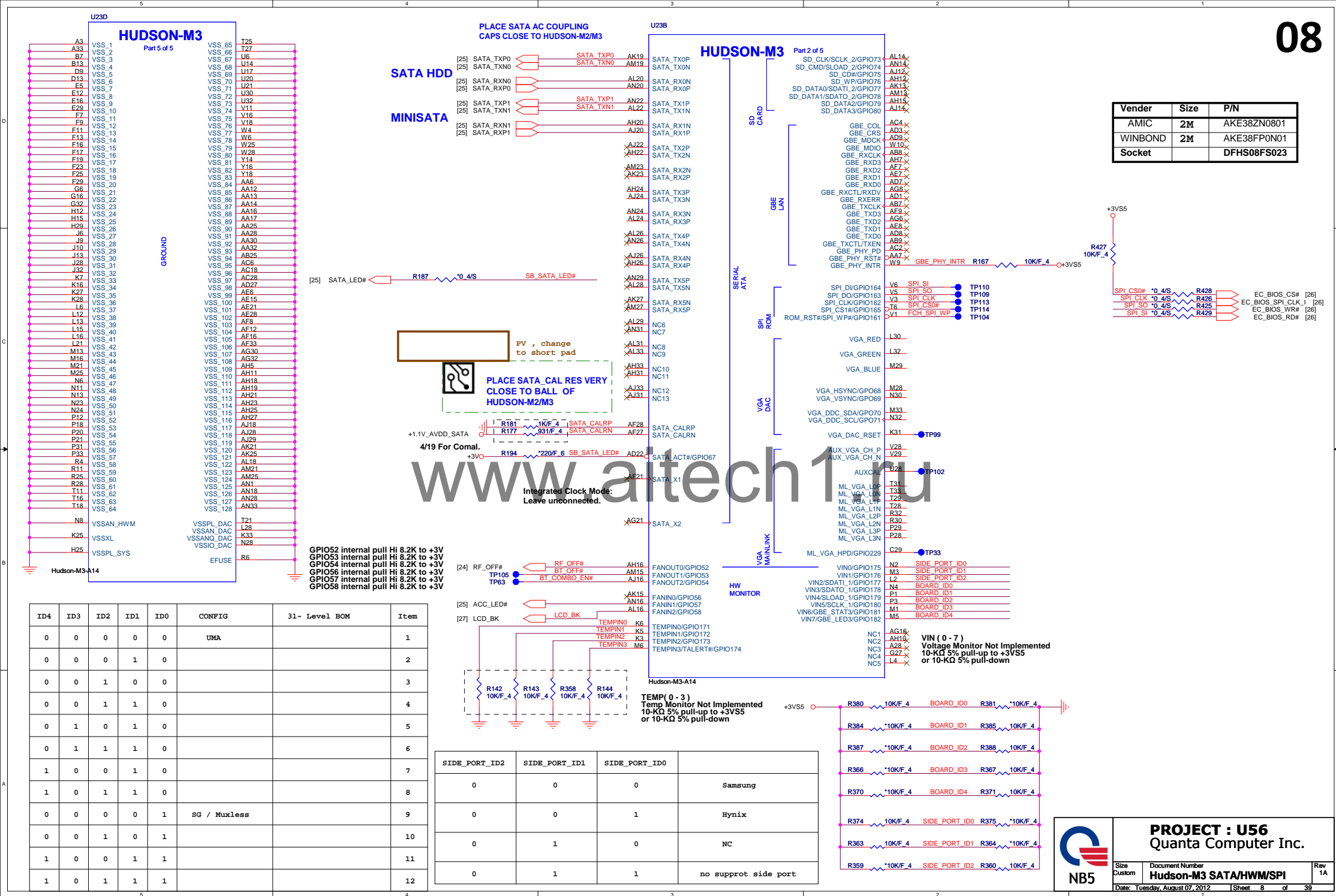
GEVENT16# internal pull Hi 8.2K to +3V55
GEVENT15# internal pull Hi 8.2K to +3V55

To Azalia



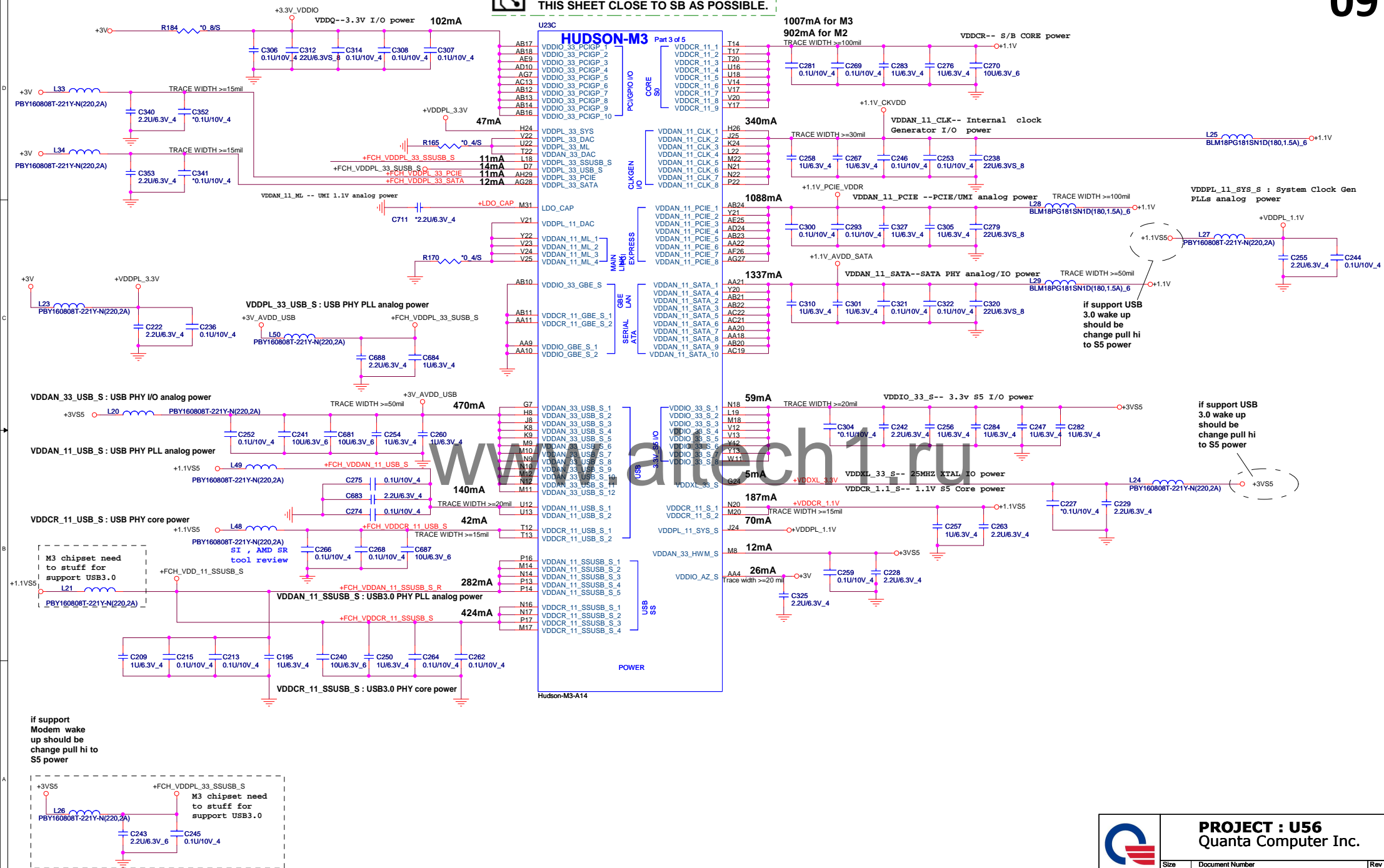
Hudson-M3-A14





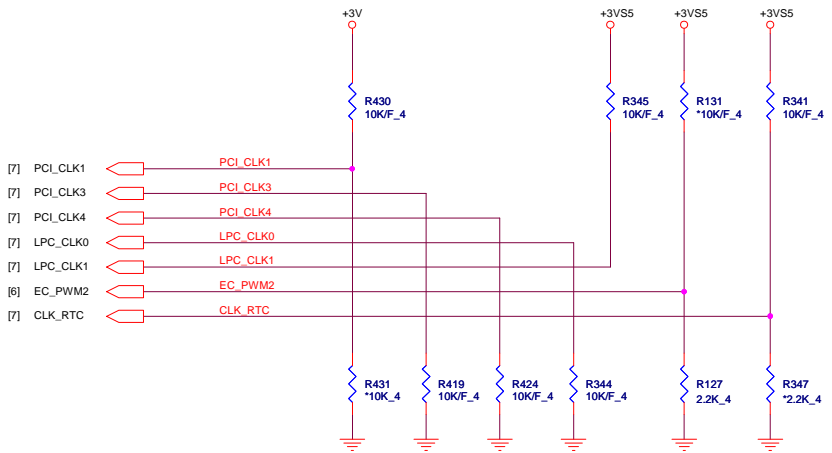


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

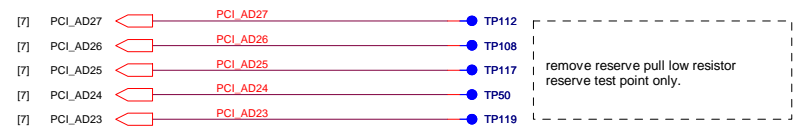


REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT

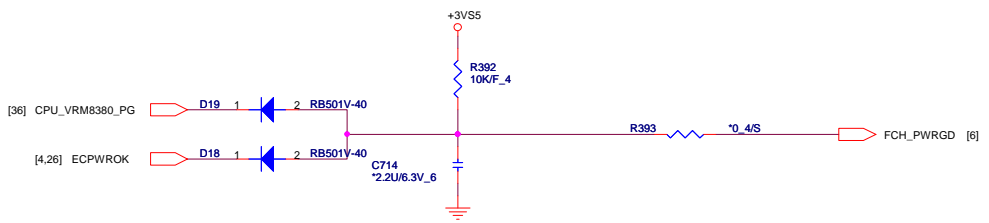
DEBUG STRAPS

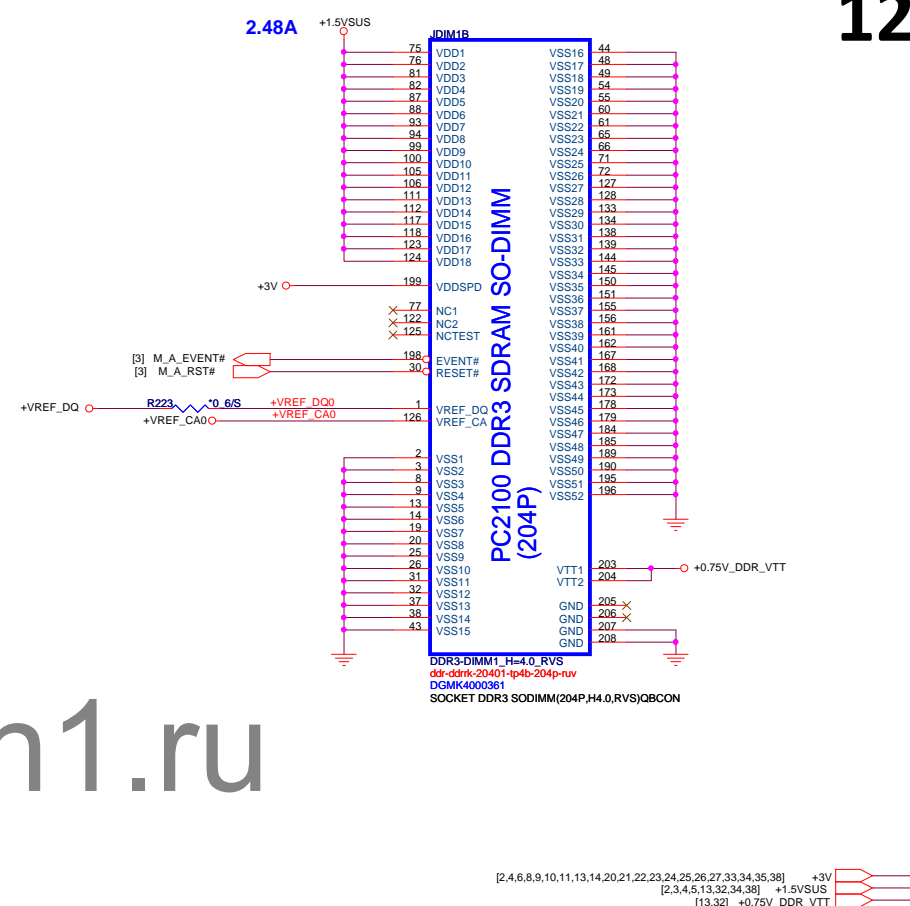
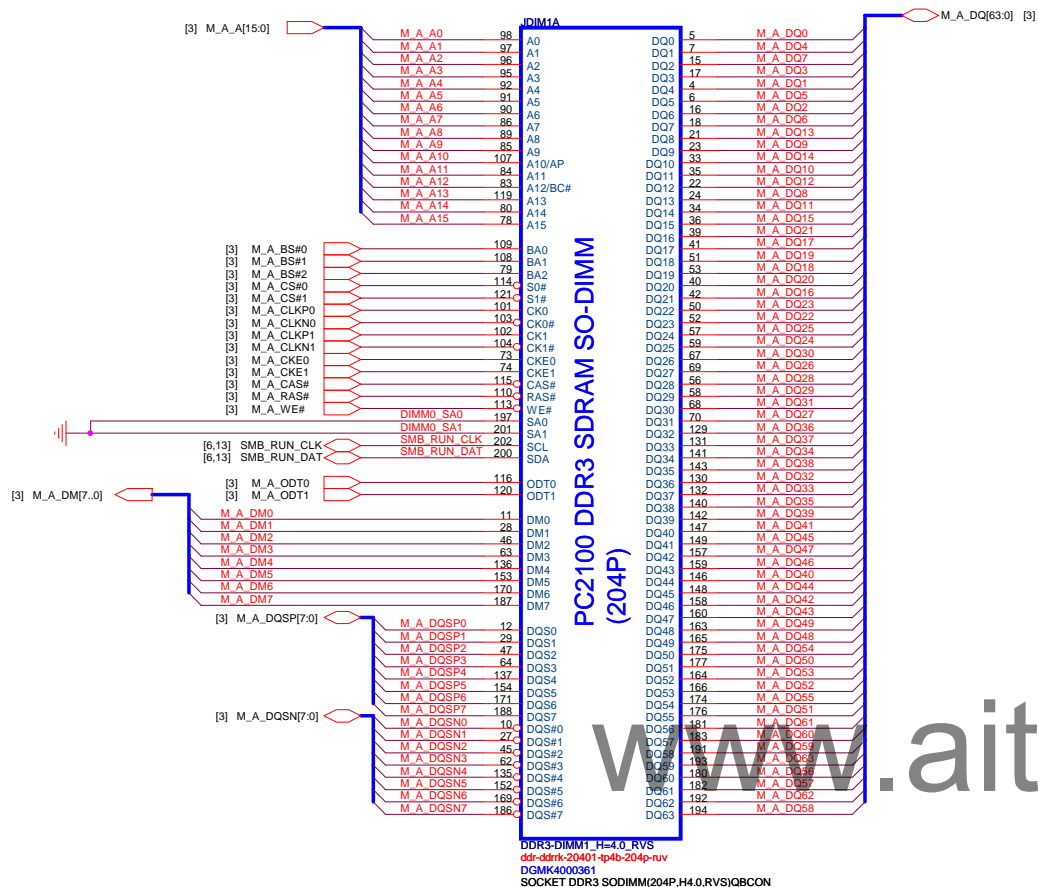
FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

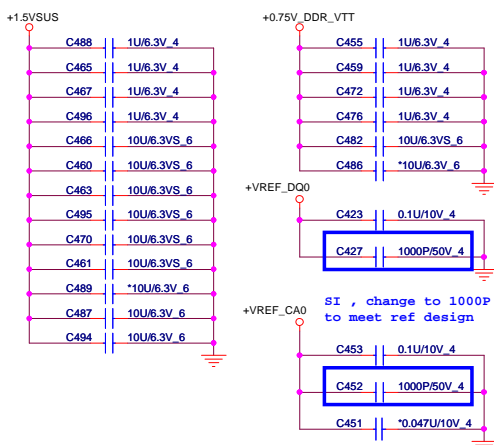
FCH_PWRGD



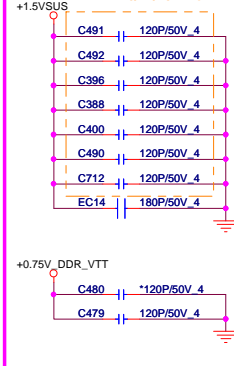


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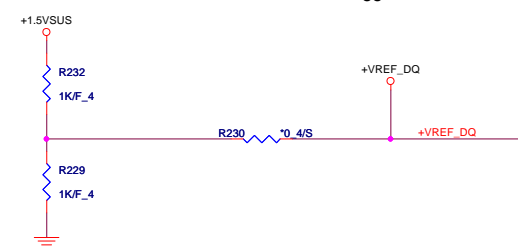
Place these Caps near So-Dimm0.

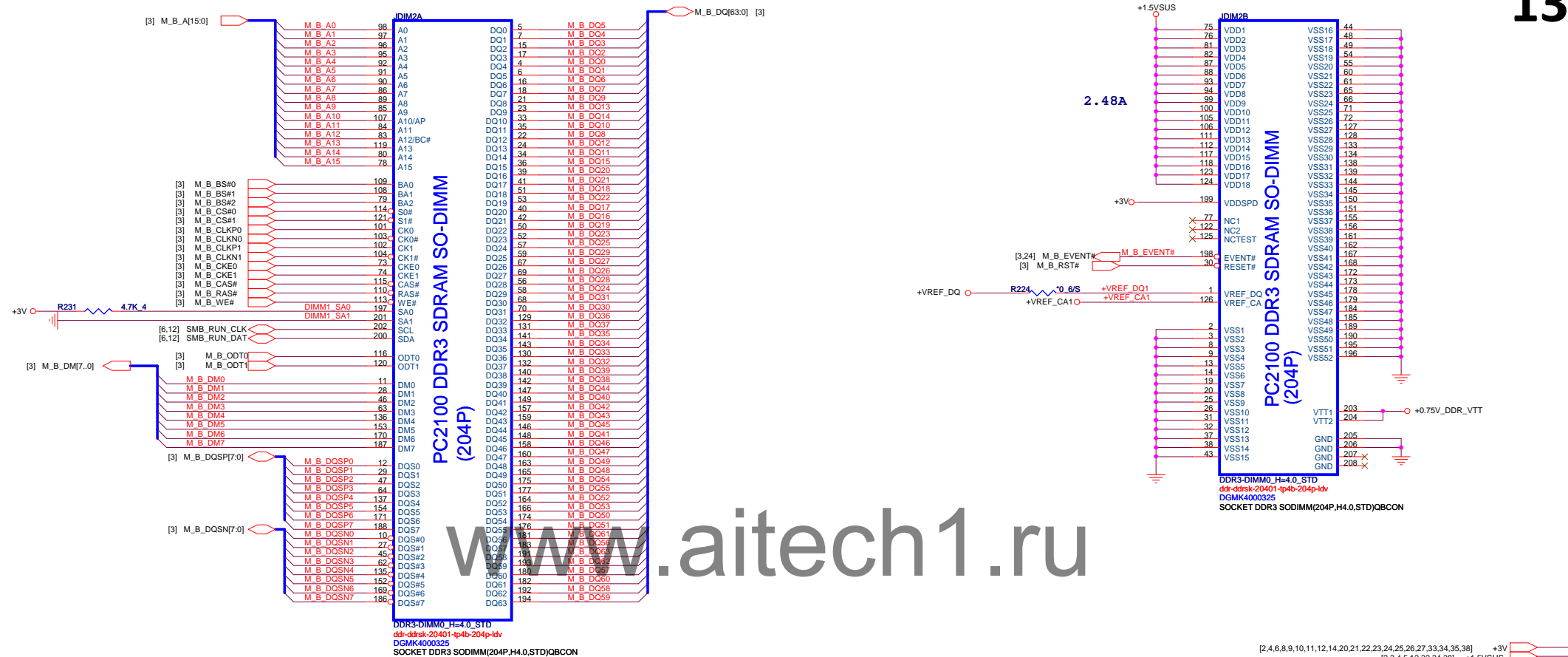


For EMI RESERVE

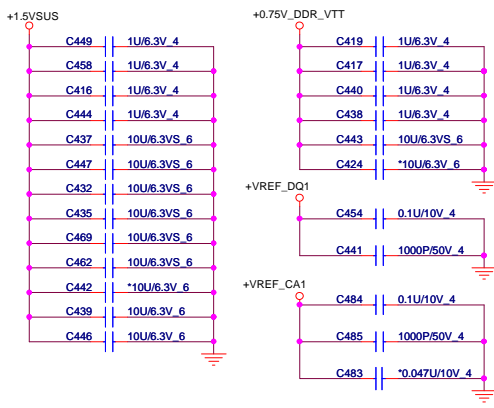
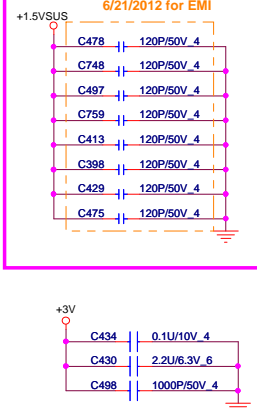


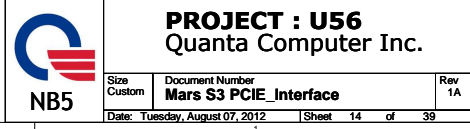
Reserved for AMD suggest



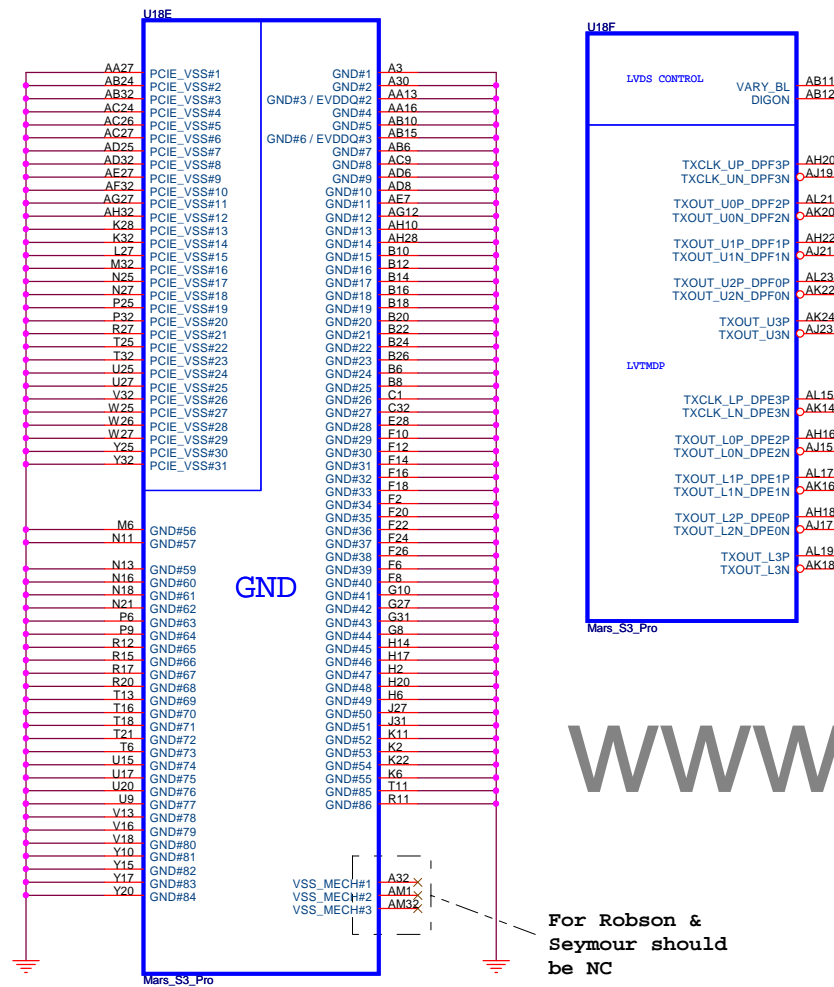


Place these Caps near So-Dimm1.

For EMI RESERVE
6/21/2012 for EMI







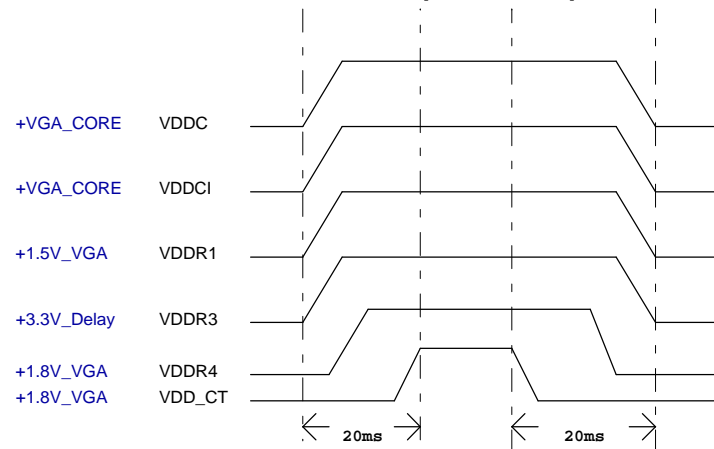
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

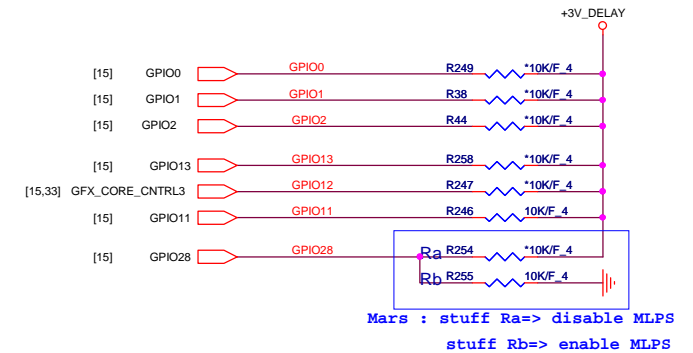
Power Up/Down Sequence



Memory Aperture size

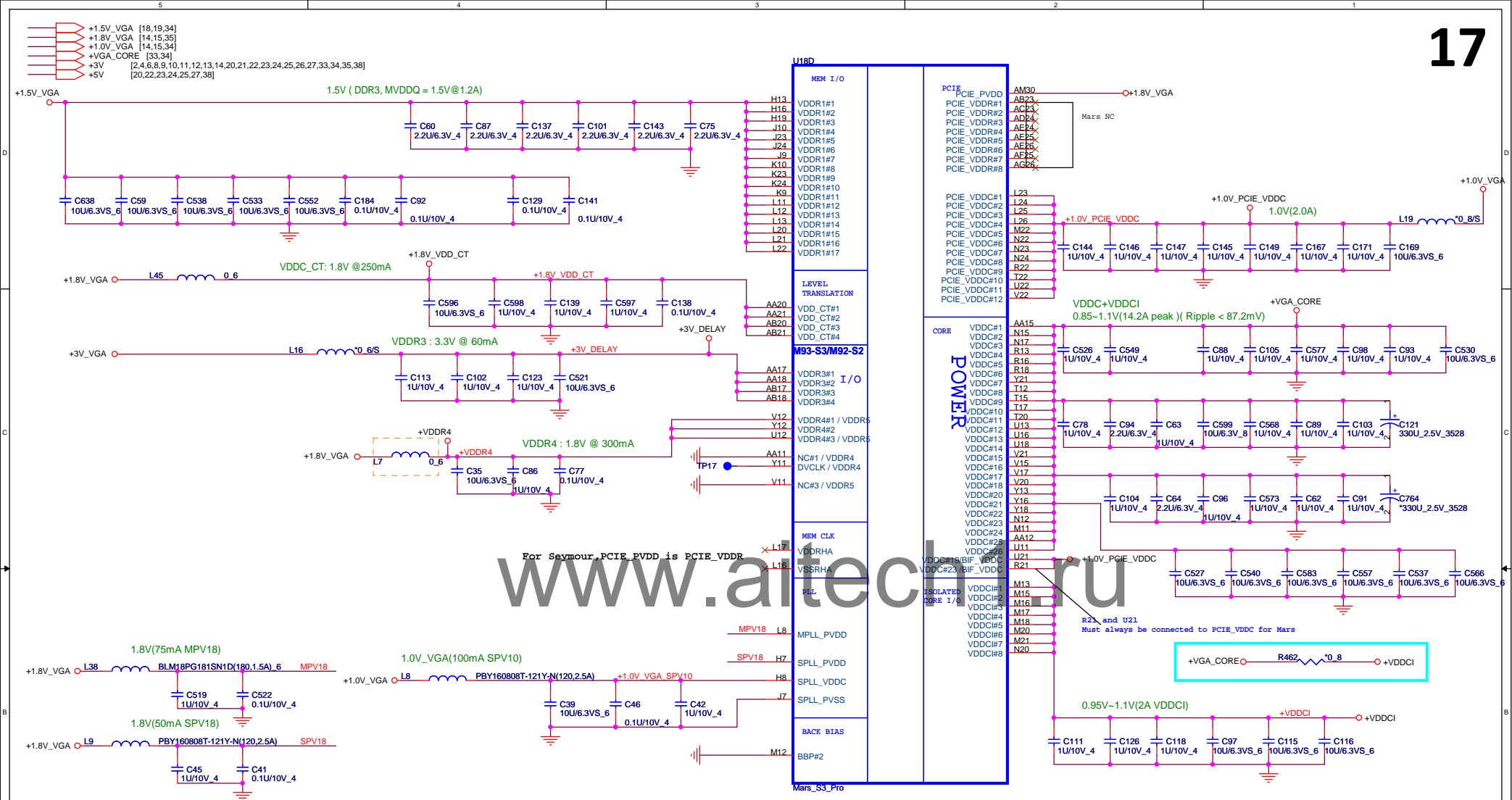
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

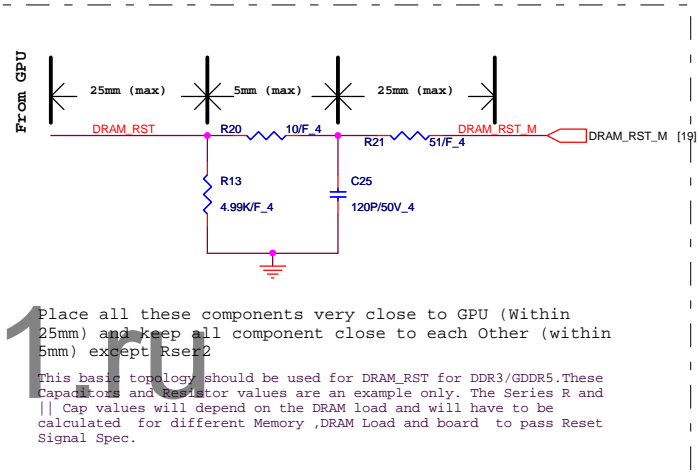
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

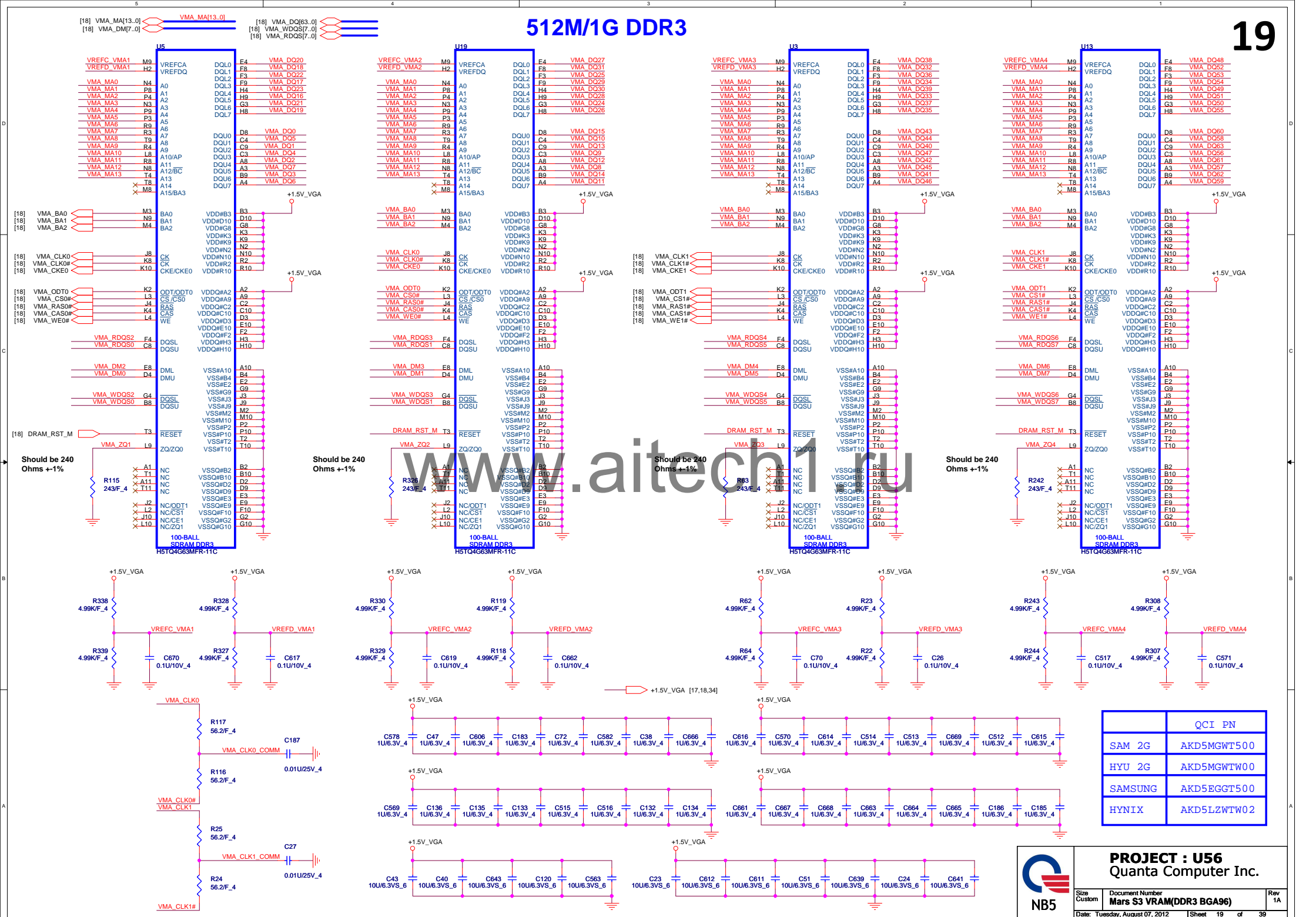


PROJECT : U56
Quanta Computer Inc.

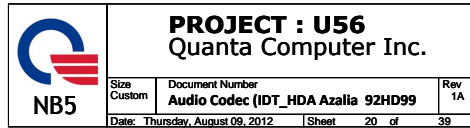
Size Custom	Document Number Mars S3 GND / LVDS/ Straps	Rev 1A
Date: Tuesday, August 07, 2012	Sheet 16 of 39	



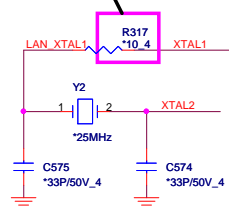




	QCI PN
SAM 2G	AKD5MGWT500
HYU 2G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZWTW02

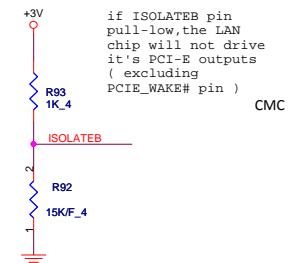
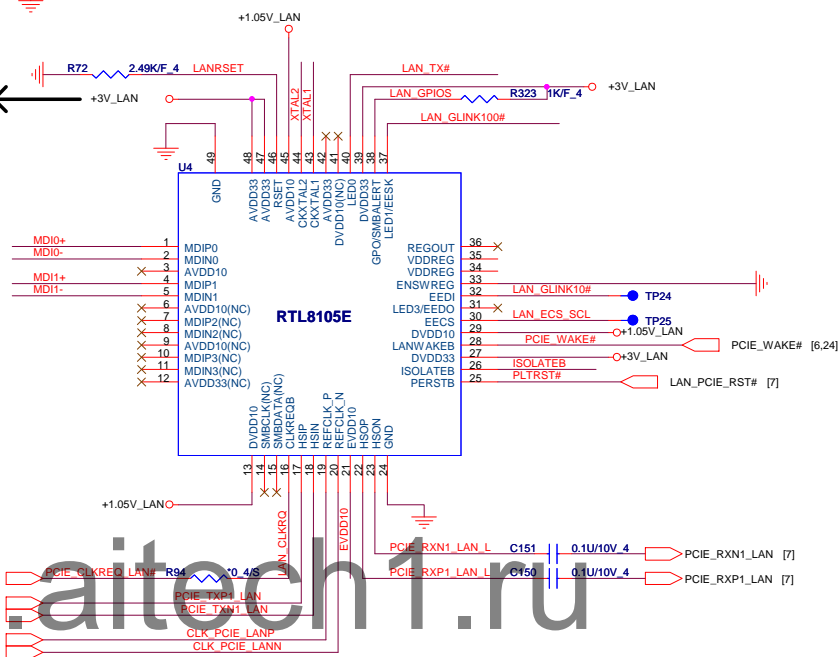
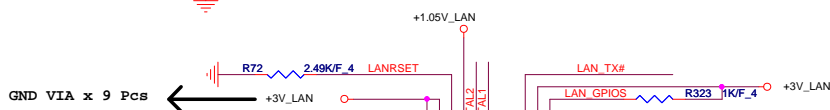
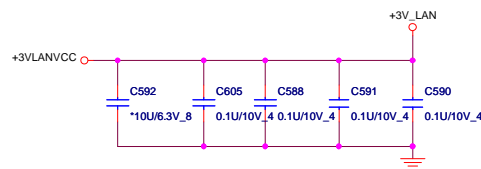
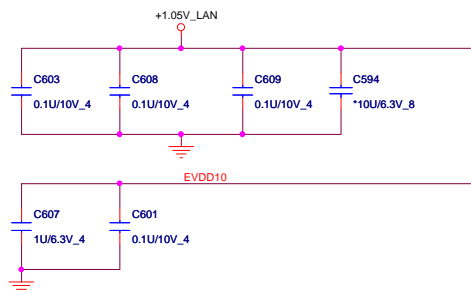
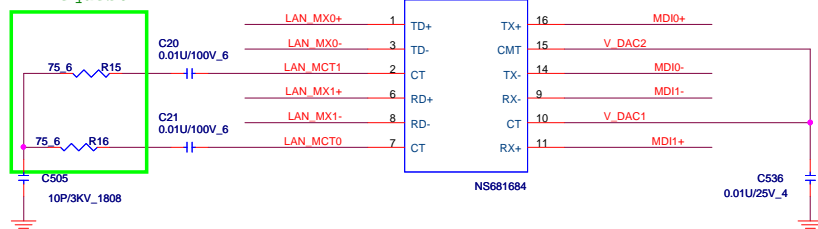


For EMI 0 ~ 22 ohm

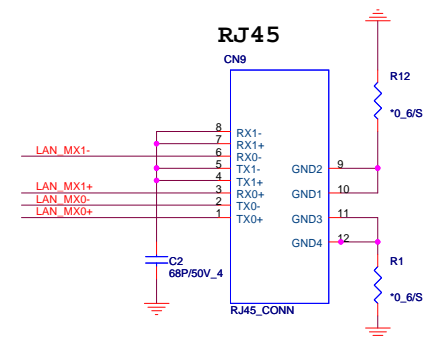
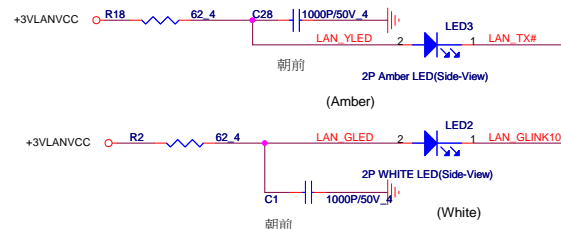


Green Clk [24] LAN_XTAL25_IN R315 510F 4 XTAL2

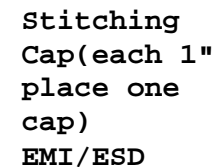
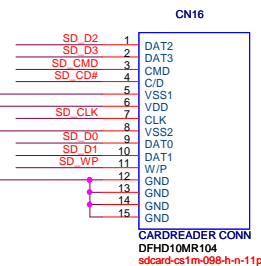
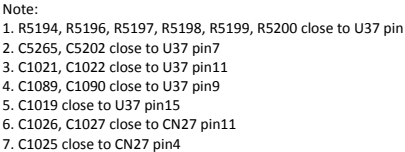
Change to 0603 size for EMI request



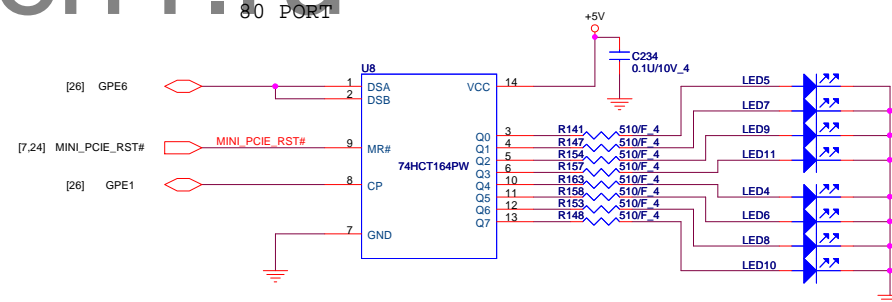
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SD / MMC

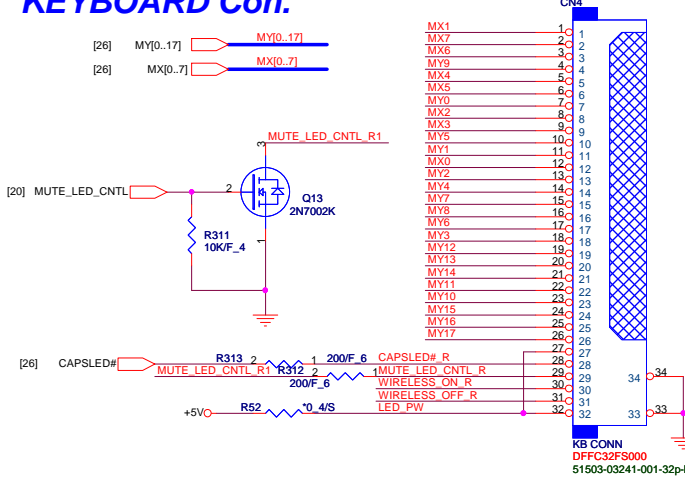


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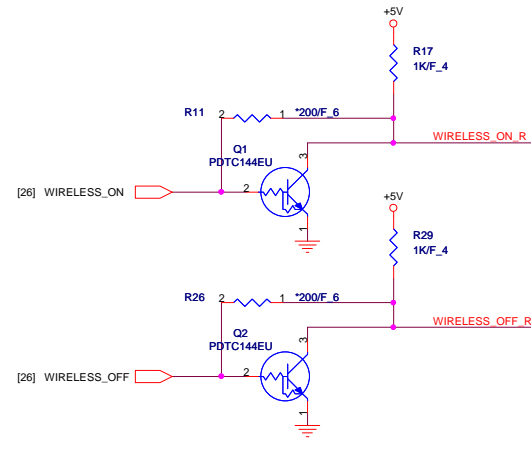
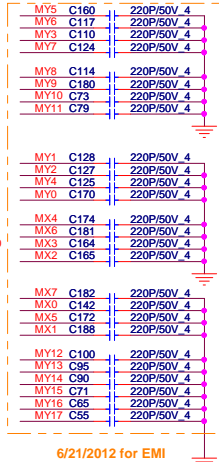
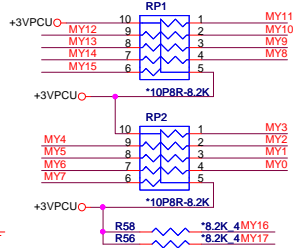


KEYBOARD Con.

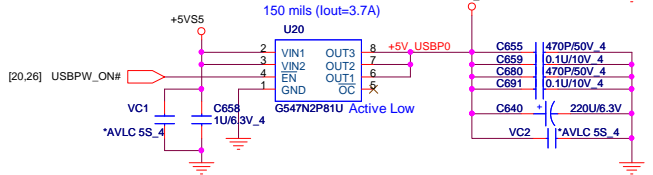
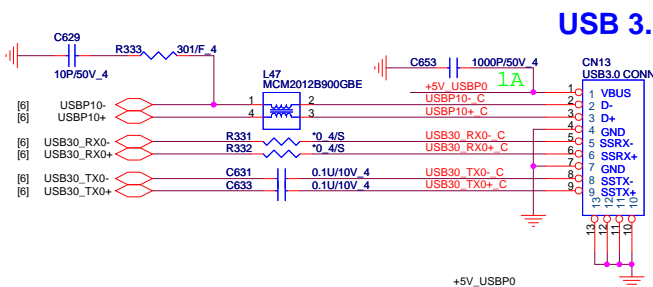
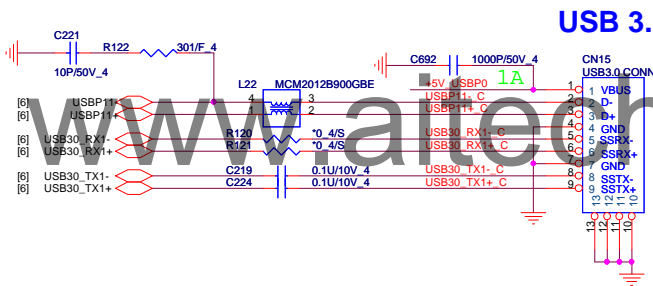
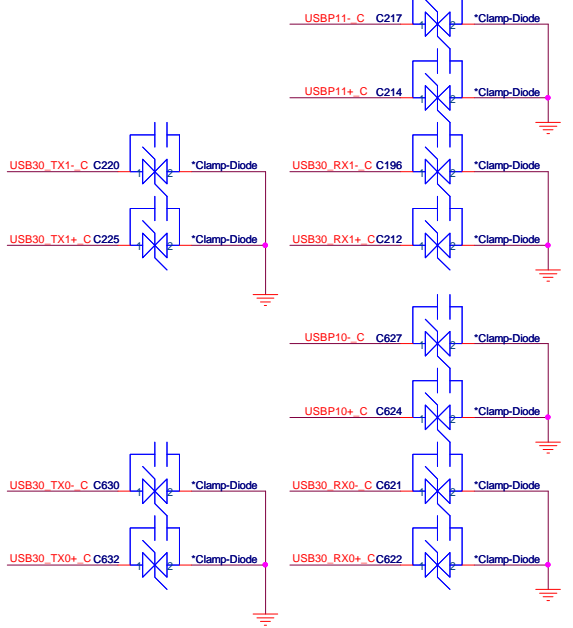
23



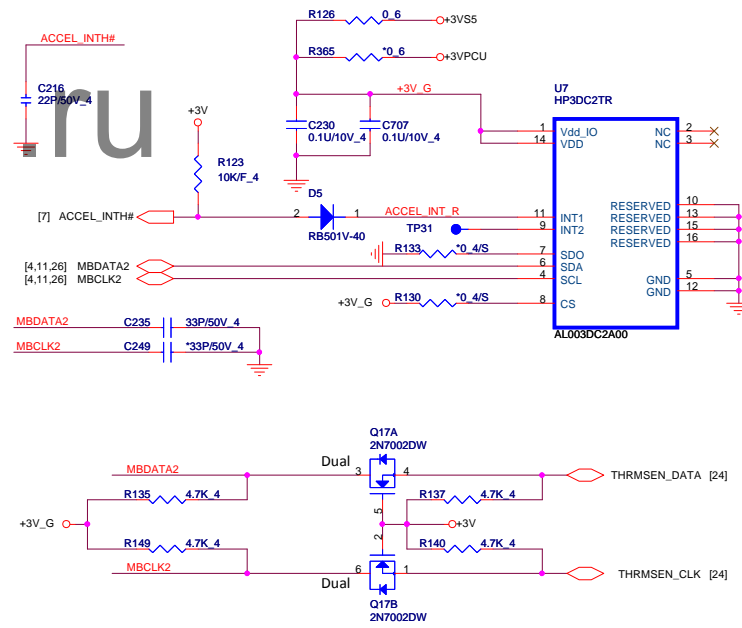
KEYBOARD PULL-UP



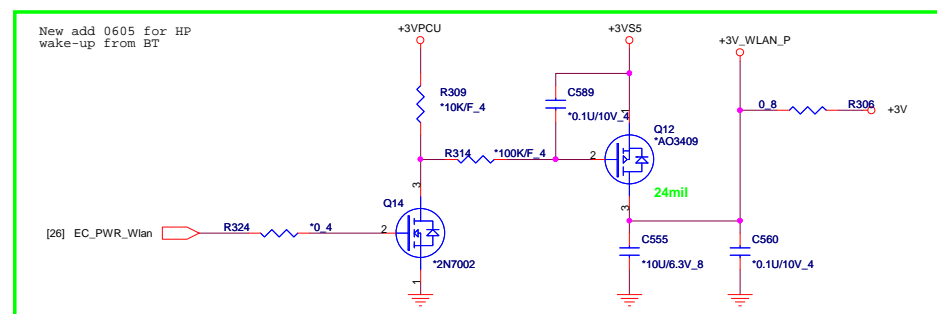
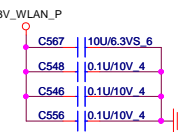
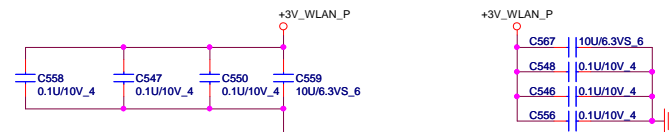
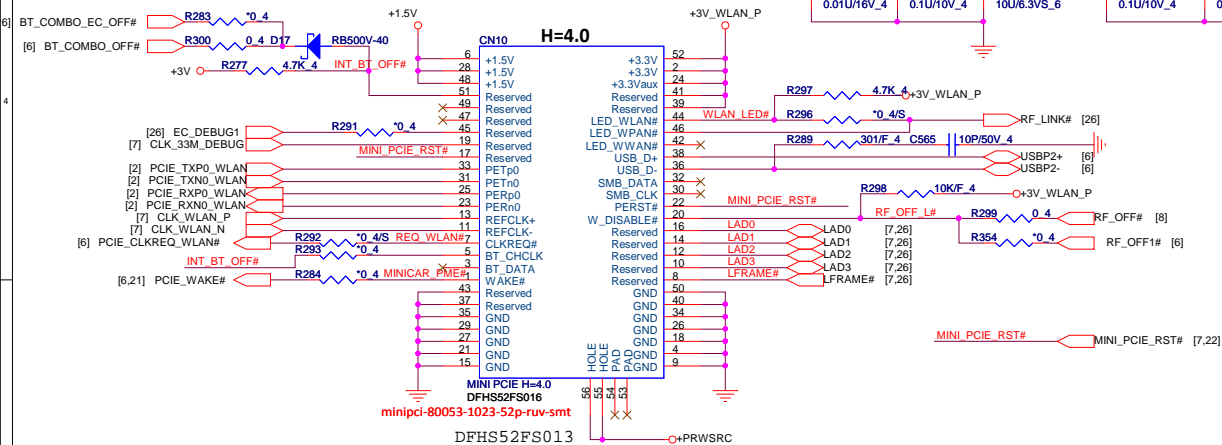
USB 2.0/3.0 Combo



Accelerometer Sensor

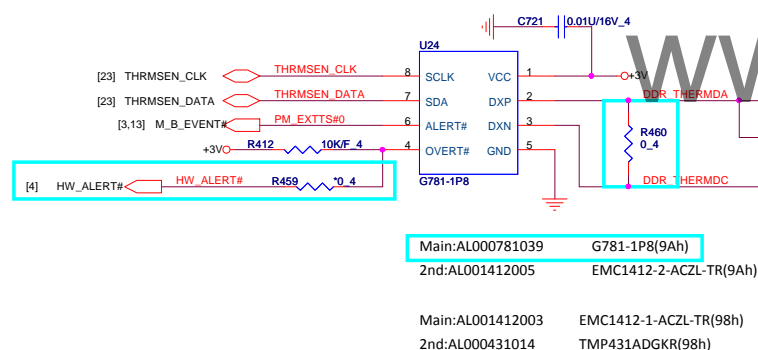


**Mini Card
WLAN/BT(Optional)**

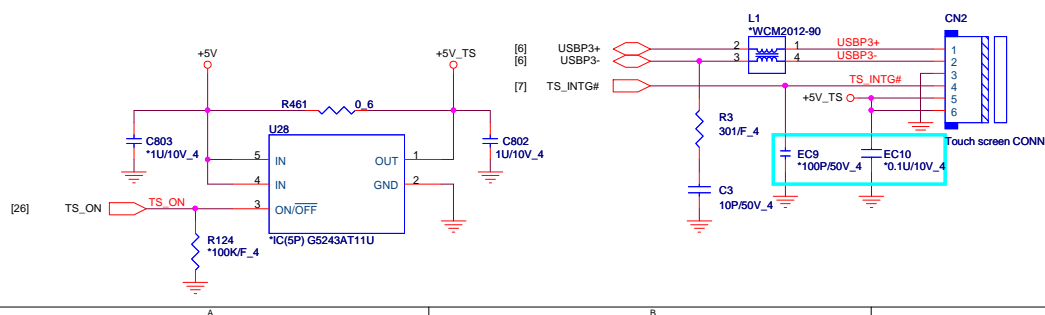


Local Thermal Sensor

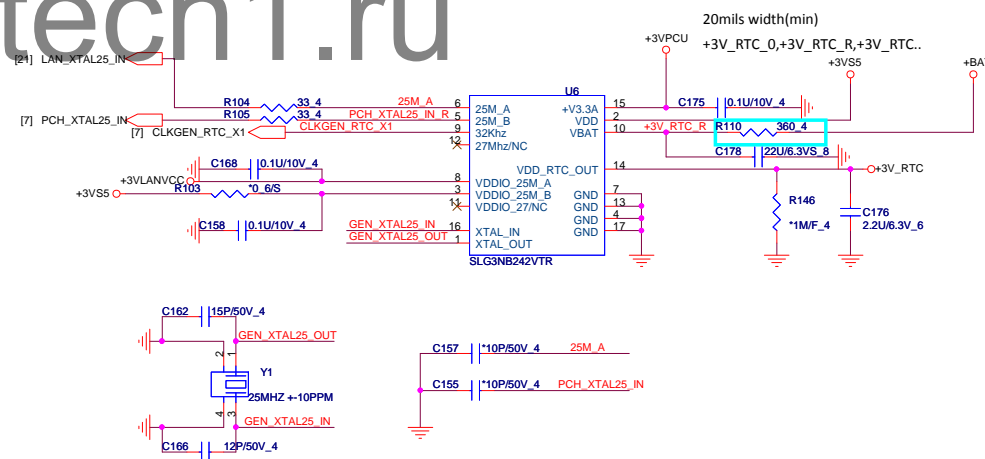
DDR3 Thermal Sensor



Touch screen

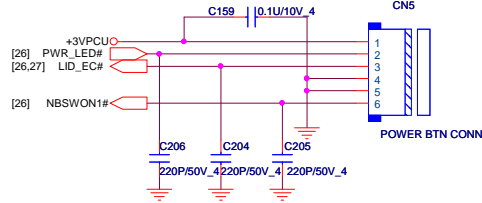


Green CLK Circuitry

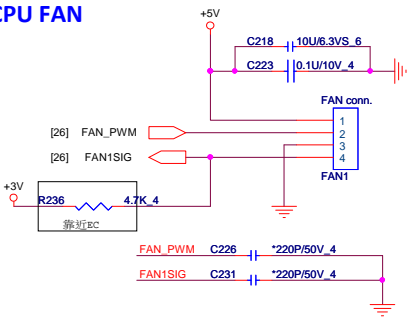


Power Button Connector

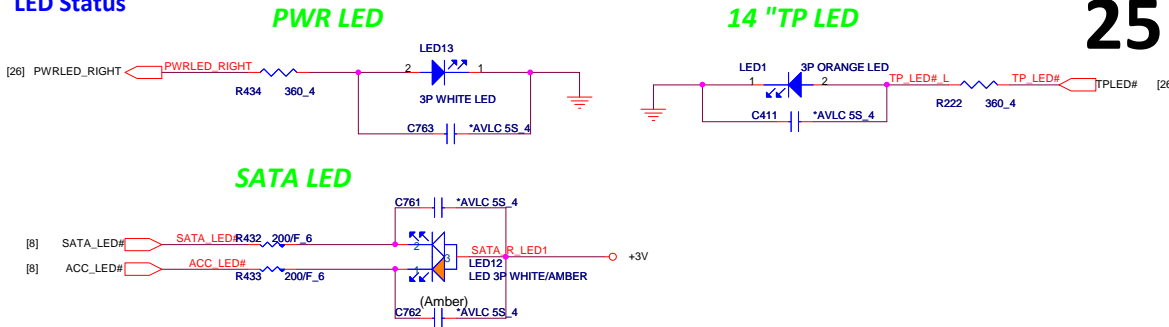
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



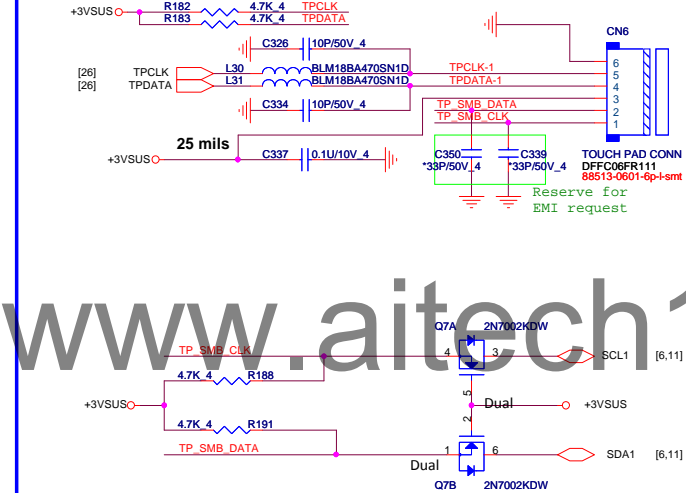
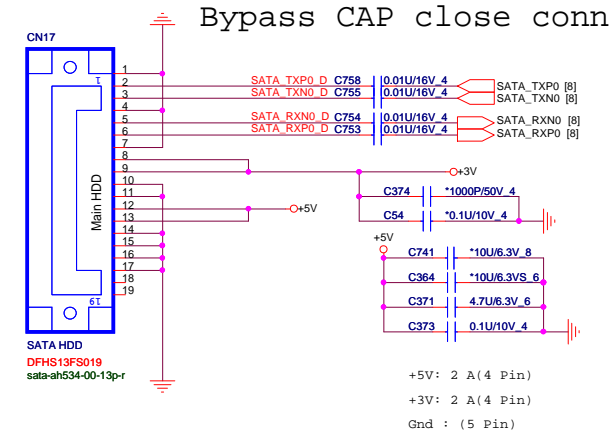
CPU FAN



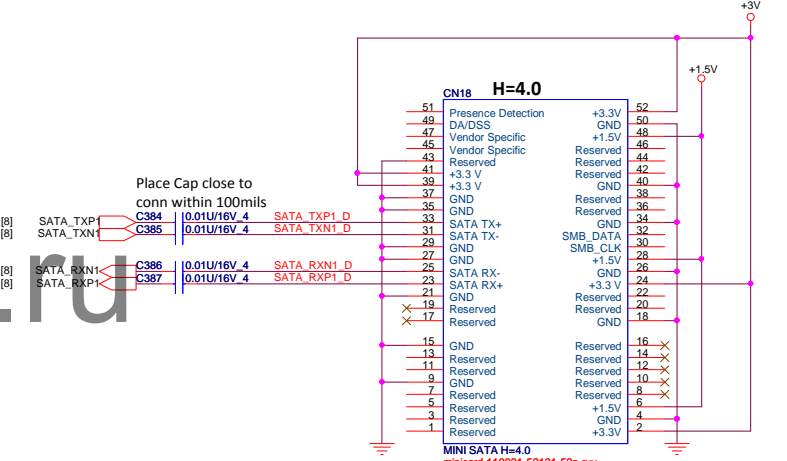
LED Status



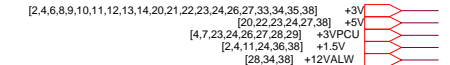
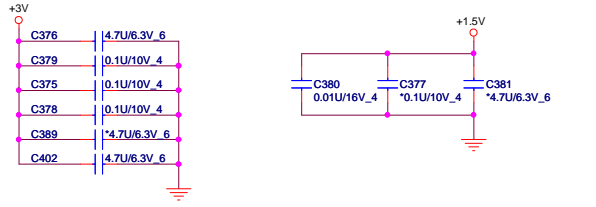
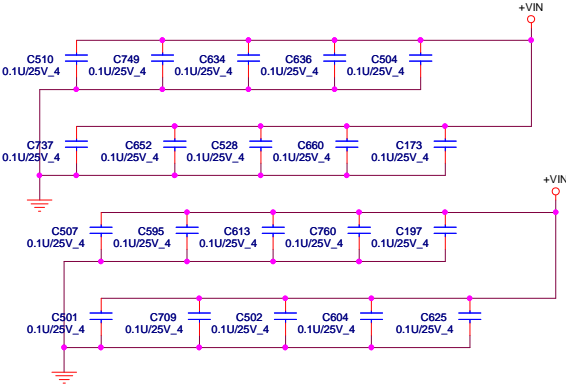
SATA HDD Connector(Cable type)



Mini PCI-E Card 2- Full size mSATA



+VIN Cap

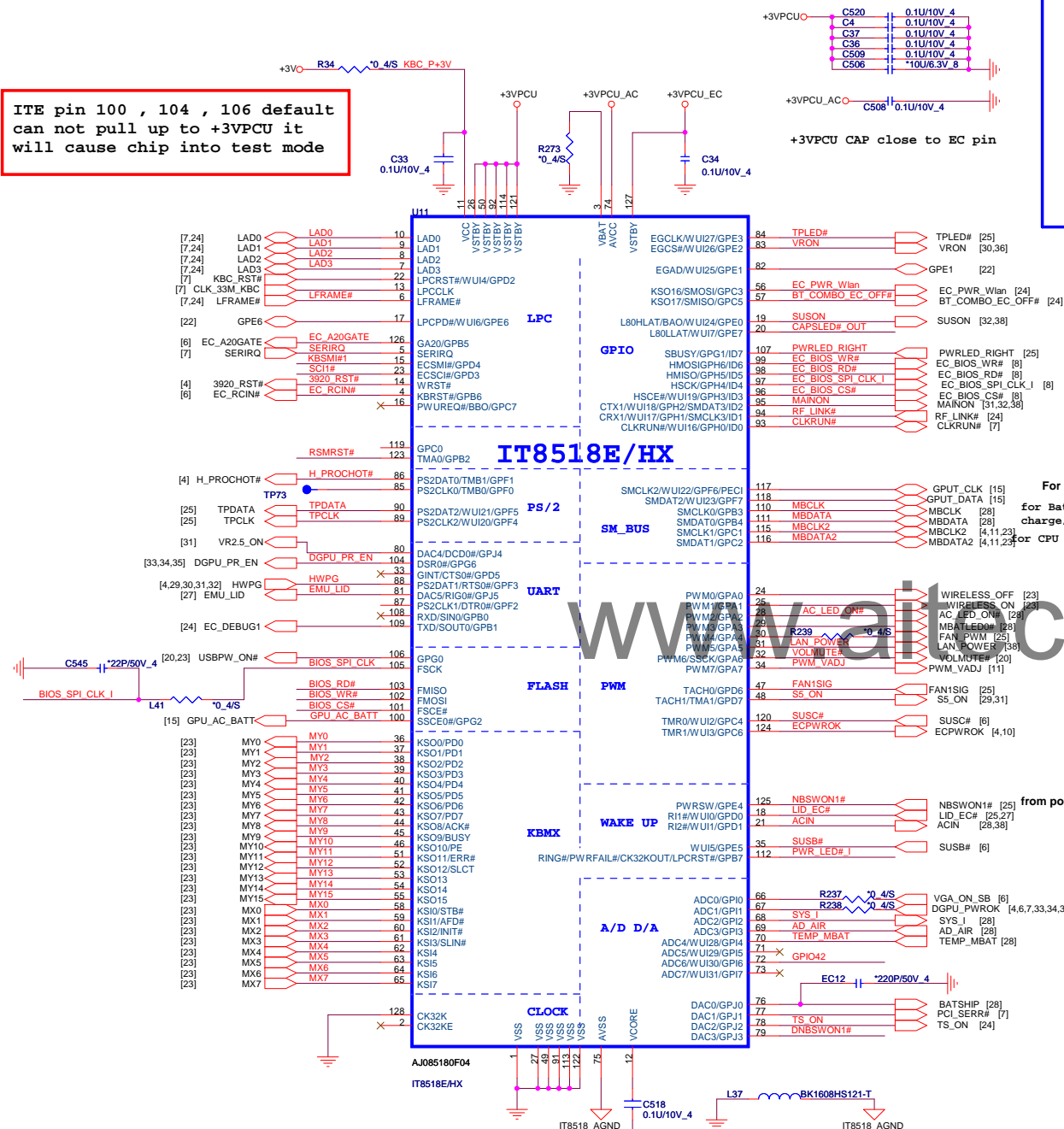


[2,4,6,8,9,10,11,12,13,14,20,21,22,23,24,25,27,33,34,35,38]

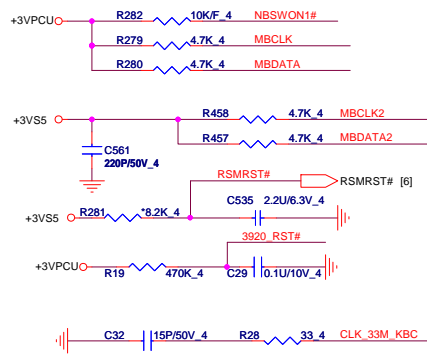
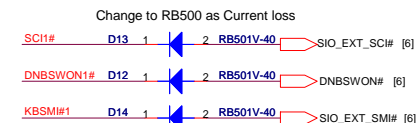
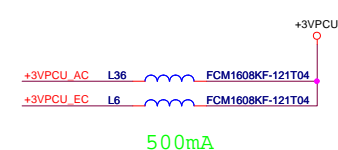
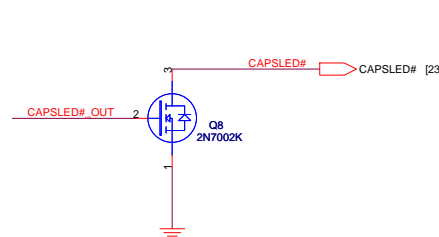
[4,7,23,24,25,27,28,29]

+3V
+3VPCU

ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode

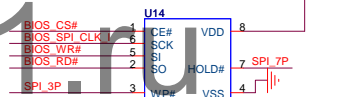


CAPS LED

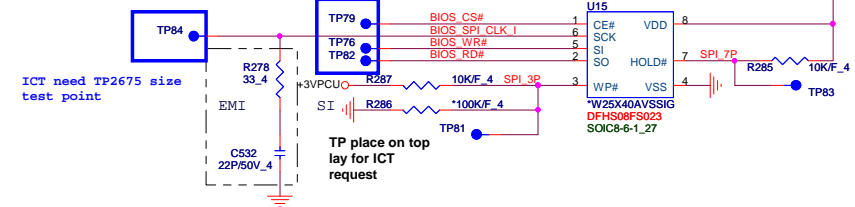


Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZNOQ02
Socket		DFHS08FS023

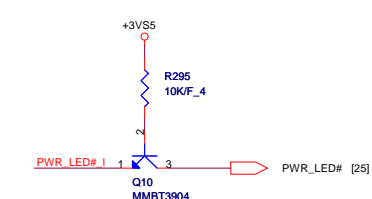
4M SPI EC ROM



128K byte SPI EC ROM



PWR_LED



Adapter select

+3VPCU R240 *10K/F_4 GPIO42 R241 10K/F_4

Hi ==> DIS/SG
Low ==> UMA

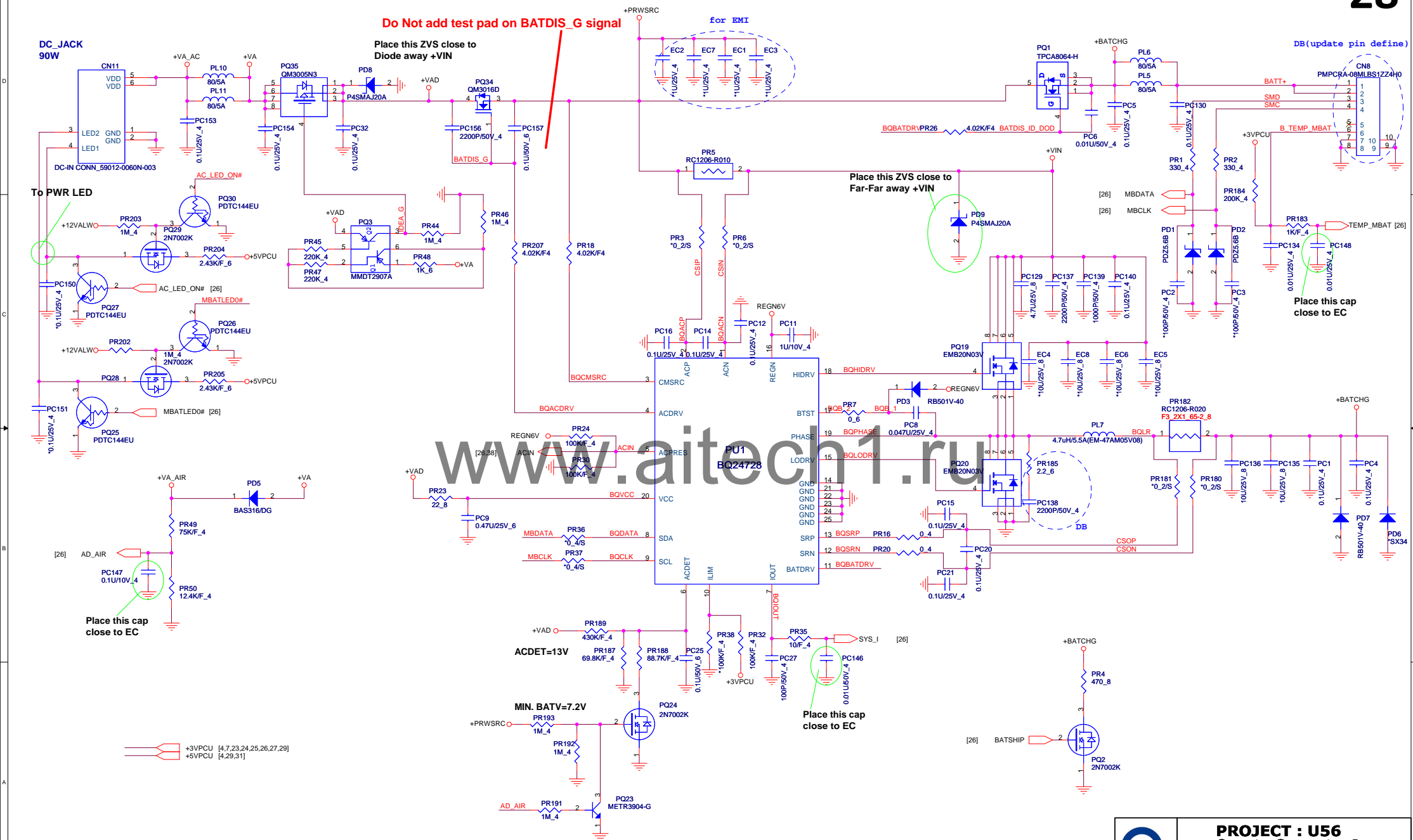
Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

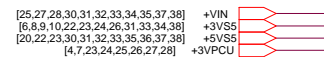


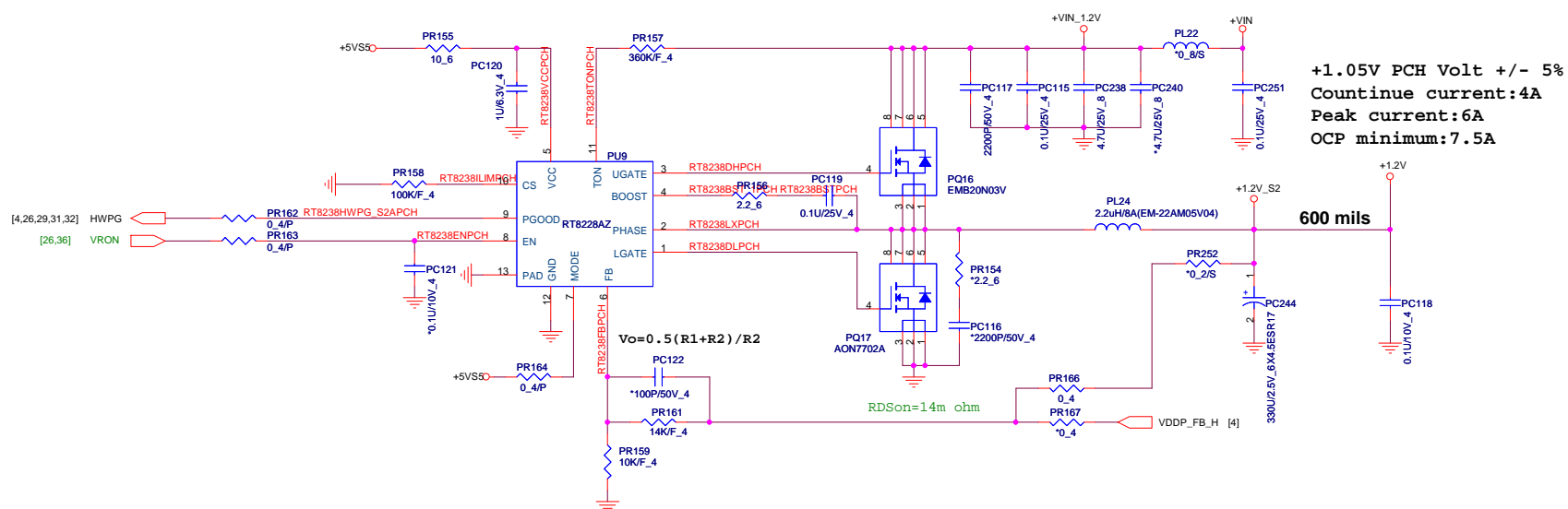
PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

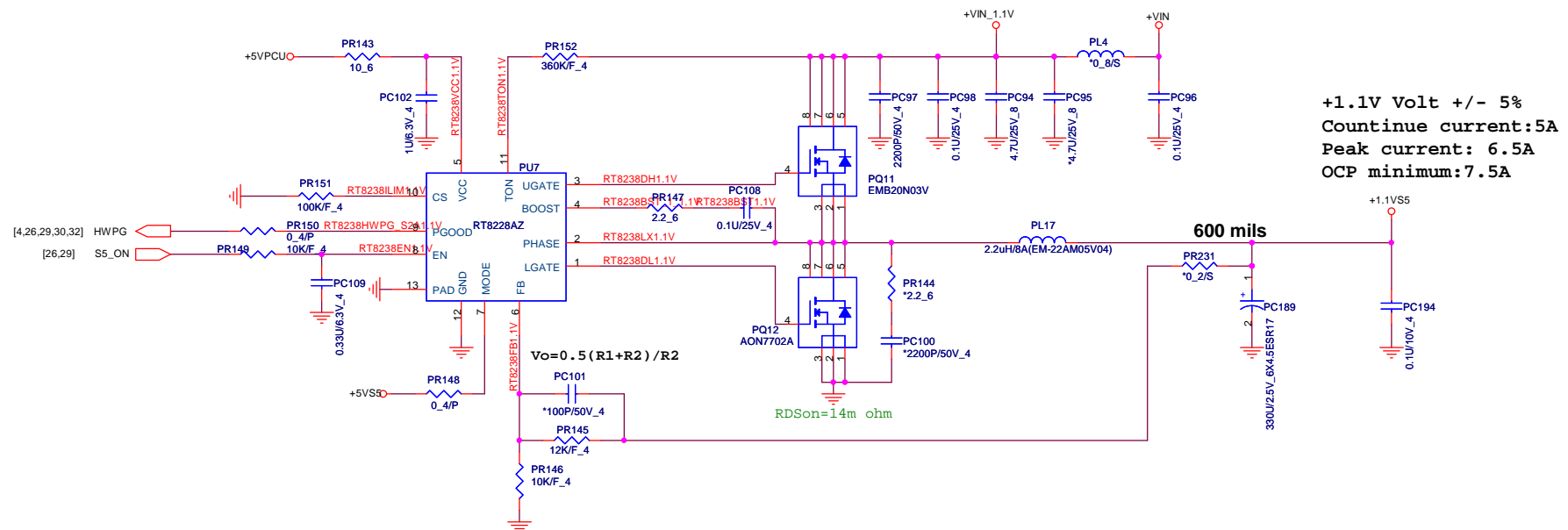
Date: Thursday, August 09, 2012 Sheet 26 of 39



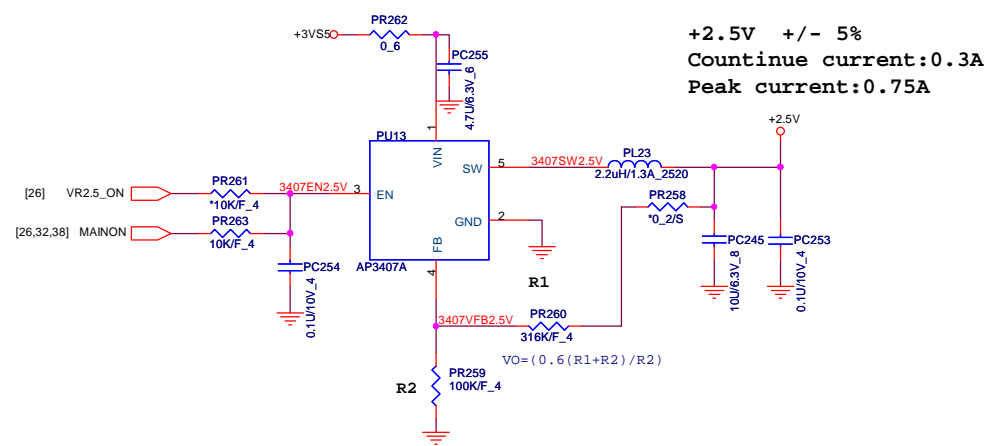


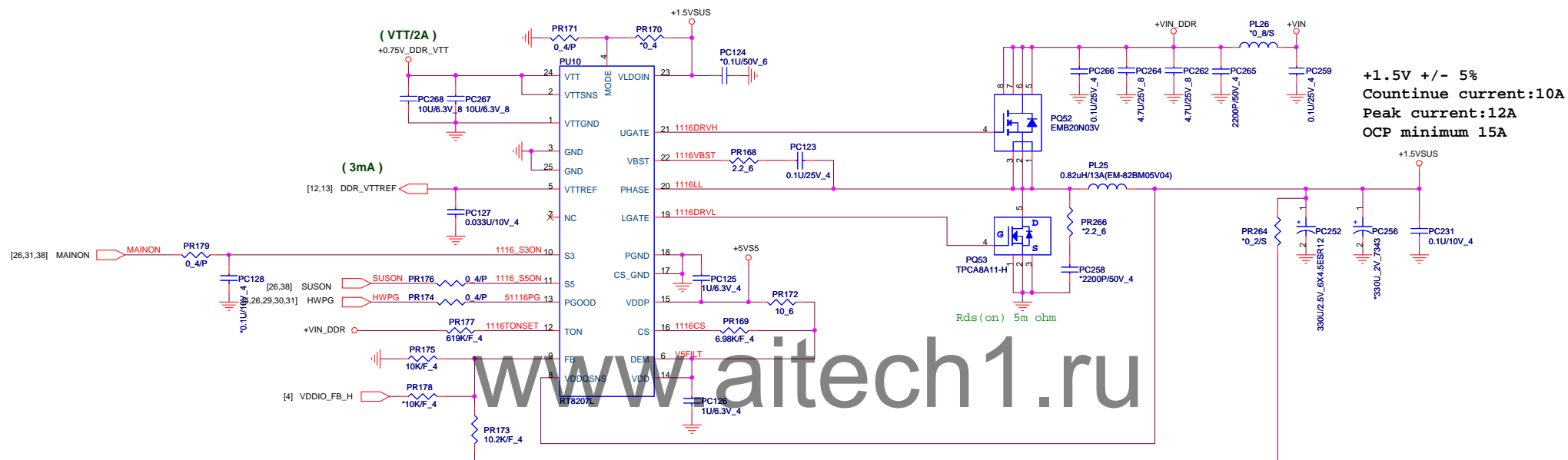


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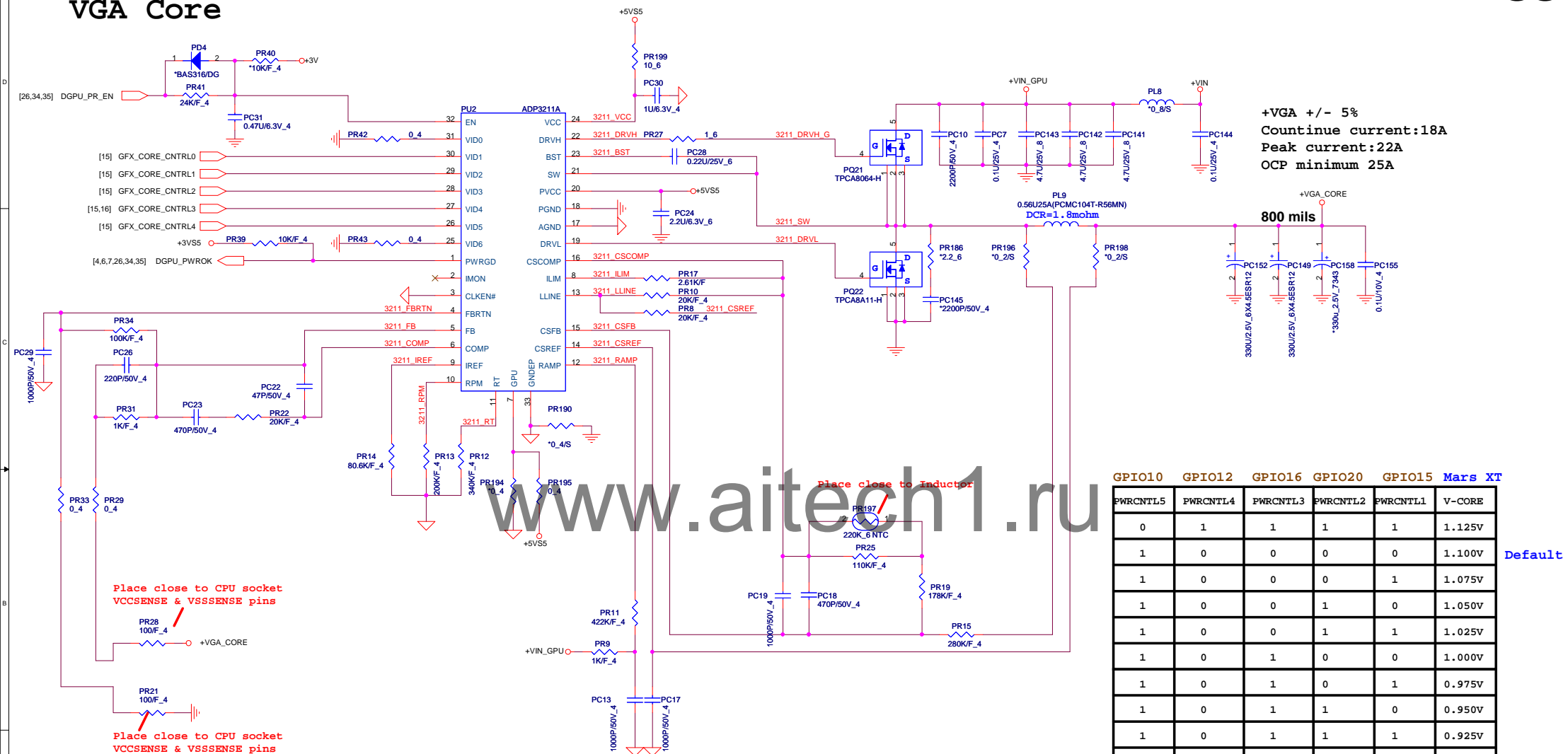


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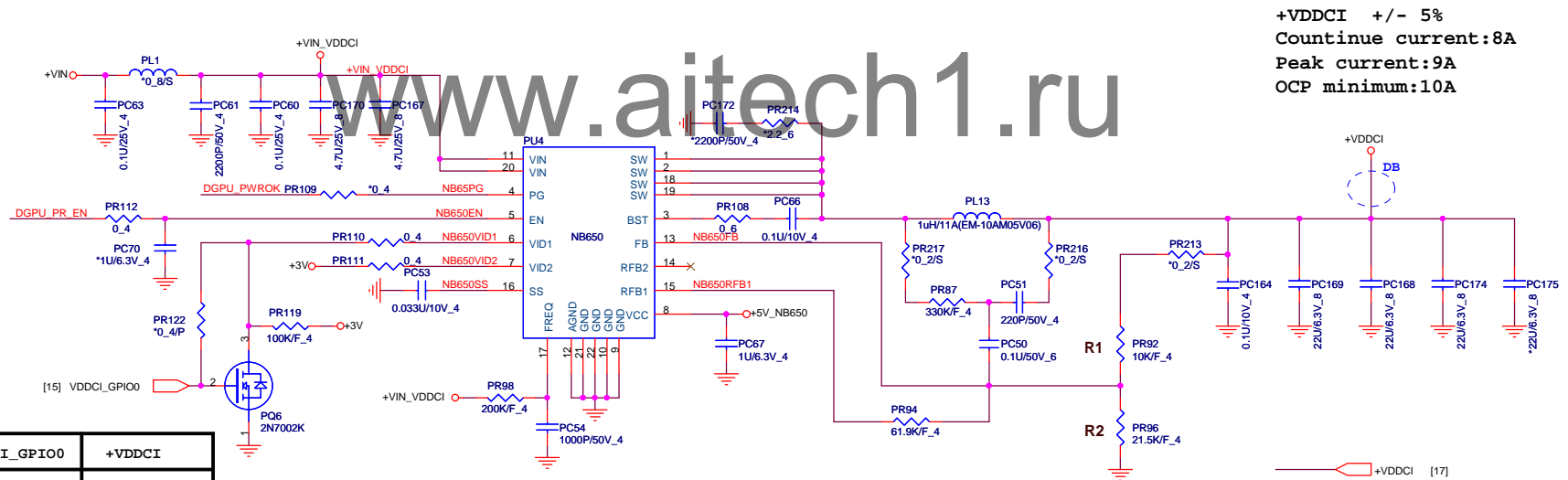
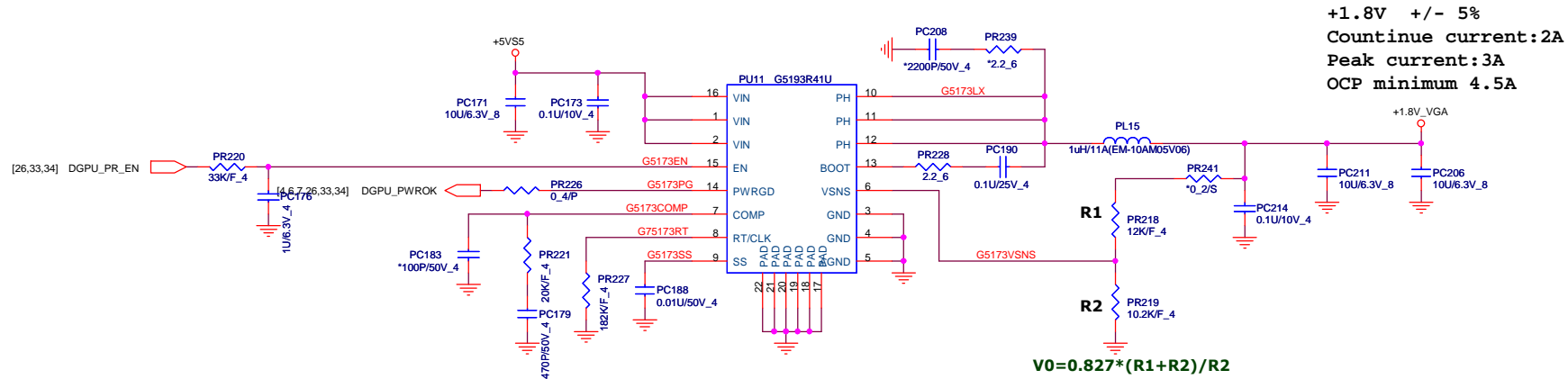




VGA Core



GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Mars XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

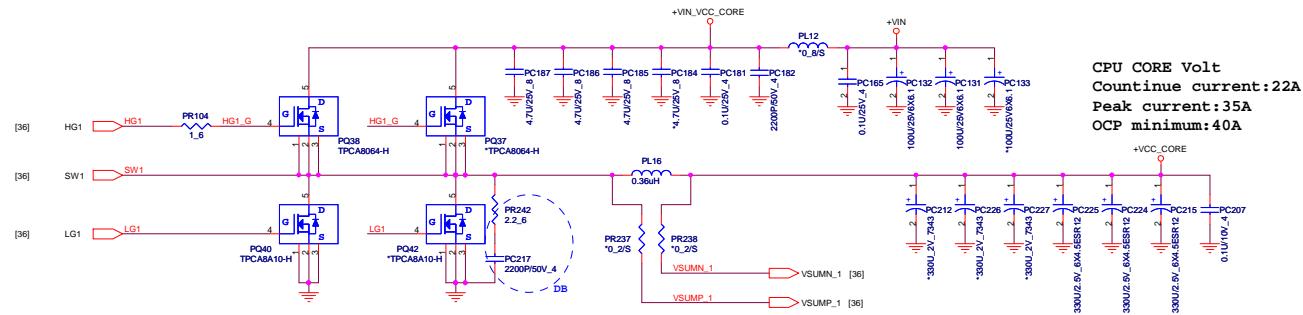


VDDCI_GPIO1	VDDCI_GPIO0	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

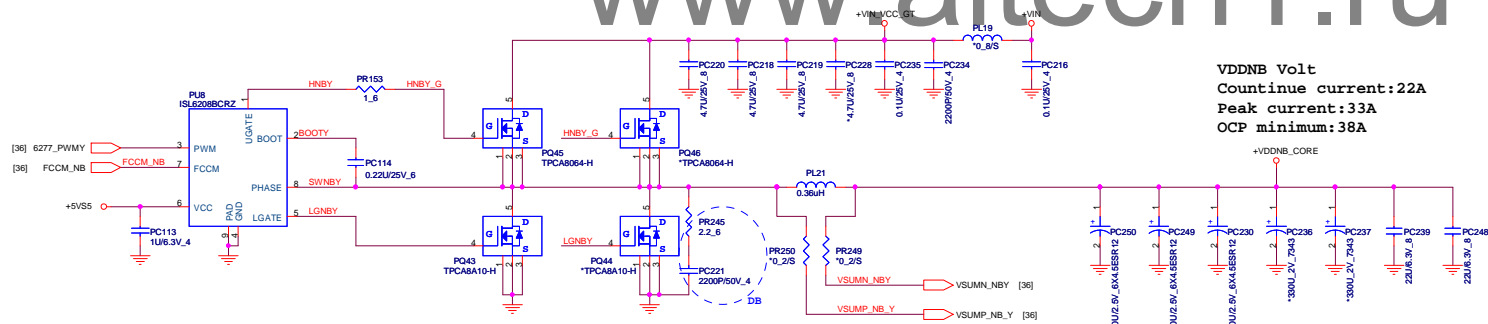


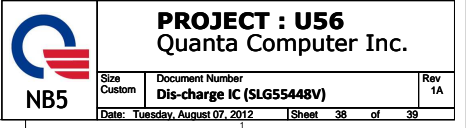
PROJECT : U56
Quanta Computer Inc.





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